KL-1501

Technical Documentation
Up / Down-Counter
24VDC, 100kHz

Please keep for further use !

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Italics and **bold** type are used for the title of a document or to emphasize text passages.

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"< >" refers to keys on your computer keyboard (e.g. <RETURN>).

Note

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Note:
The cover of this document shows the current revision status and the corresponding date. Since each individual page has its own revision status and date in the footer, there may be different revision statuses within the document.

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Revision	Date

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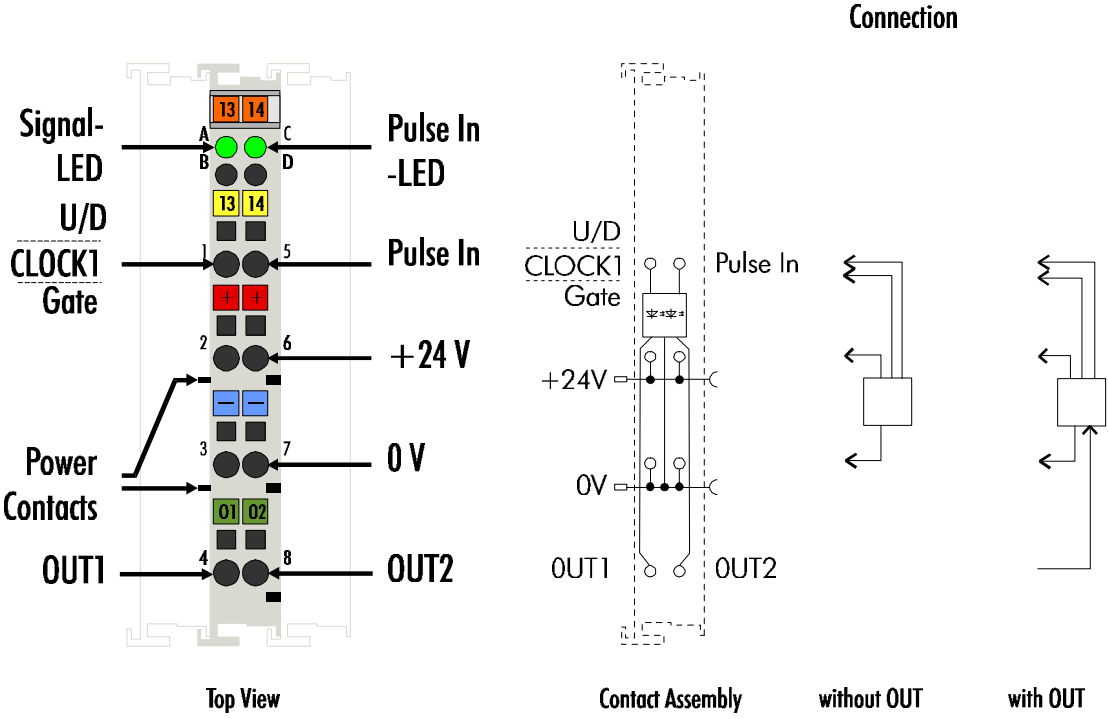
24 V DC, 100 kHz Up/Down-Counter KL-1501



Technical Data	KL-1501
Number of inputs	1 / 2
Rated load voltage	24 V DC (20 V ... 29 V)
´0´signal voltage	-3 V ... 5 V
´1´signal voltage	15 V ... 30 V
Switching frequency	100 kHz
Input current	5 mA. typ.
Current consumption from T-Bus	50 mA typ.
Counter depth	32 Bit
Electrical isolation	500 Vrms (T-Bus / field voltage)
Bit widtth in the process image	48 I/O: 32 bits data, 8 bits control/status, 8 bits not used
Configuration	no address settings, configuration via T-Bus
Weight approximately	50 g
Operating temperature	0°C ... +55°C
Storage temperture	-25°C ... +85°C
Relative humidity	95% no condensation
Vibration/shock resistance	In accordance with IEC 68-2-6 / IEC 68-2-27
EMC resistance burst/ESD	In accordance with EN 61000-4-4 / EN 61000-4-2 Limits to EN 50082-2
Installation position	any
Degree of protection	IP20

Description of functions

The input terminal KL-1501 counts birnary pulses and transmits the current value to the higher-level control system. In addition to the 32-bit up/down counter, a 32-bit gated counter or two 16-bit counters is/are available as operating modes. In the gated counter mode, a low level (high level also configurable as from software version 2A) at the V/R input suppresses the terminal's counting function. If two 16-bit counters are active, the V/R input is the clock input for the second counter. Two digital outputs can also be set.
The maximum input frequency is limited to 100 kHz. The minmum pulse width of the input signal is approximately 1 microsecond. The counters react to the rising edge of the input signal.
Via the control byte, from the control system the counter status can be set, the terminal's counting function can be suppressed and the outputs can be activated. An internal function can also be activated to enable automatic setting of the outputs at defined counter statuses.

Version note

Up to December 20, 1996 (production date: week 49), the terminal KL-1501 was supplied in the gated counter mode and in the alternative output format. The current setting of the terminal is as an up/down counter in the standard output format (32-bit counter).

LED display

The LEDs indicate the states of the V/R and CLOCK inputs as well as the states of the outputs A0 and A1.

Process data

Standard output format

When using the standard output format, 5 bytes (4 bytes of user information data and 1 control/status byte) are mapped. The process data differs depending on the set function:

- Gated counter:
  32-bit unsigned integer
- Up/down counter:
  32-bit signed integer
- Two active counters:
  2*16-bit unsigned integer

Mapping of the terminal in the standard format is described in further detail in the section on terminal configuration.

Alternative output format

- Up/down counter:
  24-bit signed integer
- Gated counter:
  24-bit signed integer
- Two active counters:
  1 x 8-bit counter0 and 1 x 16-bit counter1

If the alternative output format is chosen, pay attention to the fact that the output length (4 bytes or 6 bytes instead of 5 bytes) and mapping of the terminal are changed.

Reference

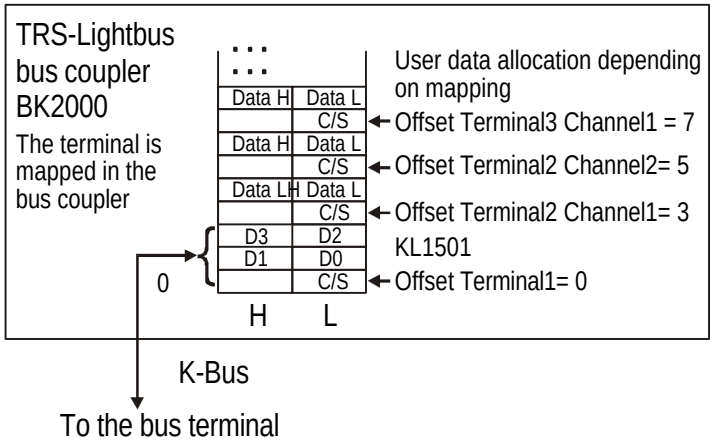
The annex contains an overview of possible mapping configurations depending on the adjustable parameters.

Terminal configuration

The terminal can be configured and parametrized by way of the internal register structure.
Each terminal channel is mapped in the bus coupler. The terminal's data is mapped differently in the bus coupler's memory depending on the type of the bus coupler and on the set mapping configuration (eg.Motorola / Intel format, word alignment,...). Contrary to the analog and output terminals, in the case of the KL-1501 the control and status byte is always also mapped, regardless of the field bus systsem used.

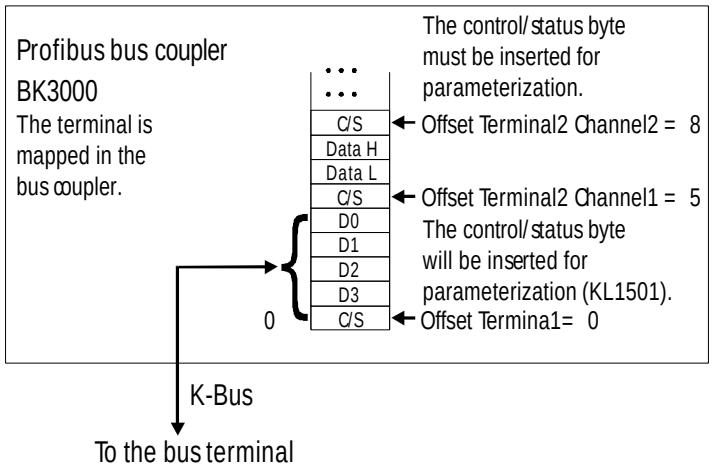
TRS Lightbus Coupler BK2000

In the case of the TRS Lightbus coupler BK2000, the control /status byte is always mapped besides the data bytes. It is always in the low byte at the offset address of the terminal channel.



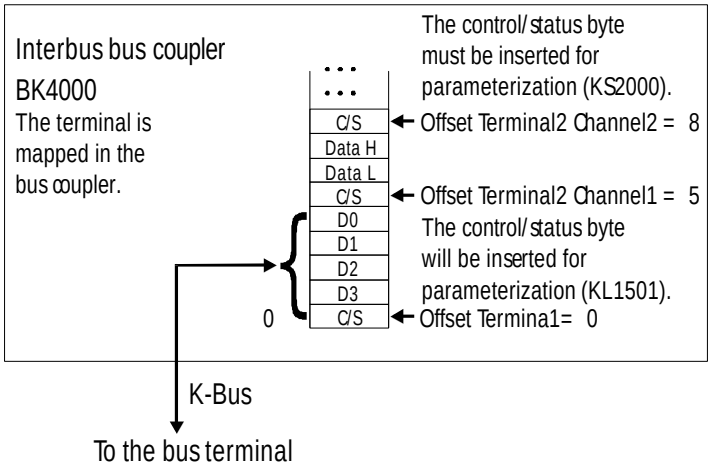
Profibus Coupler BK3000

When using the Profibus coupler BK3000, the KL-1501 is automatically mapped with 5 bytes of input data and 5 bytes of output data.



Interbus Coupler BK4000

By default, the Interbus coupler BK4000 maps the KL-1501 with 5 bytes of input data and 5 bytes of output data.



Other bus couplers and further information

You will find further information on the mapping configuration of bus couplers in the annex of the respective bus coupler manual under the heading of "Configuration of masters".

Parametrization with the KS2000 software

Parametrization operations can be carried out independantly of the field bus system using the TRS KS2000 configuration software via the serial configuration interface in the bus coupler.

Register communication KL-1501

General register description

Complex terminals that possess a processor are capable of bidirectionally exchanging data with the higher-level control system. Below, these terminals are referred to as intelligent bus terminals. They include the analog inputs (0-10V, -10-10V, 0-20mA, 4-20mA), the analog outputs (0-10V, -10-10V, 0-20mA, 4-20mA), serial interface terminals (RS485, RS232, TTY, data transfer terminals), counter terminals, the encoder interface, the SSI interface, the PWM terminal and all other parametrizable terminals.

Internally, all intelligent terminals possess a data structure that is identical in terms of its essential characteristics. This data area is organized in words and embraces 64 memory locations. The essential data and parameters of the terminal can be read and adjusted by way of this structure. Function calls with corresponding parameters are also possible. Each logical channel of an intelligent terminal has such a structure (therefore, 4-channel analog terminals have 4 register sets).

This structure is broken down into the following areas:
(You will find a list of all registers at the end of this documentation).

Area	Address
Process variables	0-7
Type registers	8-15
Manufacturer parameters	16-31
User parameters	32-47
Extended user area	48-63

Process variables

R0 - R7 Registers in the terminal's internal RAM:

The process variables can be used in addition to the actual process image and their functions are specific to the terminal.

R0 - R5: These registers have a function that depends on the terminal type.

R6: Diagnostic register

The diagnostic register may contain additional diagnostic information. In the case of serial interface terminals, for example, parity errors that have occurred during data transfer are indicated.

R7: Command register

High-Byte_Write = function parameter
Low-Byte _Write = function number
High-Byte _Read = function result
Low-Byte_ Read = function number

Type registers

R8 - R15 Registers in the terminal's internal ROM

The type and system parameters are programmed permanently by the manufacturer and can only be read by the user, but cannot be modified.

R8: Terminal type

The terminal type in register R8 is needed to identify the terminal.

R9: Software version X.y

The software version can be read as an ASCII character string.

R10: Data length

R10 contains the number of multiplexed shift registers and their length in bits.
The bus coupler sees this structure.

R11: Signal channels

In comparison with R10, the number of logically existing channels is located here. For example, one physically existing shift register may consist of several signal channels.

R12: Minimum data length

The respective byte contains the minimum data length of a channel to be transferred. The status byte is omitted if the MSB is set.

R13: Data type register

Data type register	
0x00	Terminal without valid data type
0x01	Byte array
0x02	1 byte n bytes structure
0x03	Word array
0x04	1 byte n words structure
0x05	Double word array
0x06	1 byte n double words structure
0x07	1 byte 1 double word structure
0x08	1 byte 1 double word structure
0x11	Byte array with a variable logical channel length
0x12	1 byte n bytes structure with a variable logical channel length (eg 60xx)
0x13	Word array with a variable logical channel length
0x14	1 byte n words structure with a variable logical channel length.
0x15	Double word array with a variable logical channel length
0x16	1 byte n double words structure with a variable logical channel length

R14: not used

R15: Alignment bits (RAM)

The analog terminal is set to a byte limit in the terminal bus with the alignment bits.

Manufacturer Parameters

R16 - R30 is the area of the "Manufacturer Parameters" (SEEROM)

The manufacturer parameters are specific to each terminal type. They are programmed by the manufacturer, but can also be modified from the control system. The manufacturer parameters are stored permanently in a serial EEPROM in the terminal and are therefore not destroyed by power failures.
These registers can only be modified after setting a code word in R31.

User Parameters

R31 - R47 " Application Parameters" area (SEEROM)

The application parameters are specific to each terminal type. They can be modified by the programmer. The application parameters are stored permanently in a serial EEPROM in the terminal and cannot be destroyed by power failures. From software version 2.A, the user area is write-protected by way of a code word.

R31: Code word register in the RAM

The code word 0x1235 must be entered here to enable modification of parameters in the user area. Write protection is set if a different value is entered in this register. When write protection is inactive, the code word is returned during reading of the register. The register contains the value zero when write protection is active.

R32: Feature register

This register defines the operating modes of the terminal. For example, a user-specific scaling can be activated for the Analog I/O`s.

R33 - R47

Registers that depend on the terminal type

Extended application area R47 - R63

These registers have not yet been implemented.

Register access via process data transfer.

bit 7=1: register mode When bit 7 of the control byte is set, the first two bytes of the user data are not used for process data transfer, but are written into or read out of the terminal's register set.

bit 6=0: read
bit 6=1: write In bit 6 of the control byte, you define whether a register is to be read or written. When bit 6 is not set, a register is read without modification. The value can be taken from the input process image.
When bit 6 is set, the user data is written into a register. The operation is concluded as soon as the status byte in the input process image has assumed the same value as the control byte in the output process image.

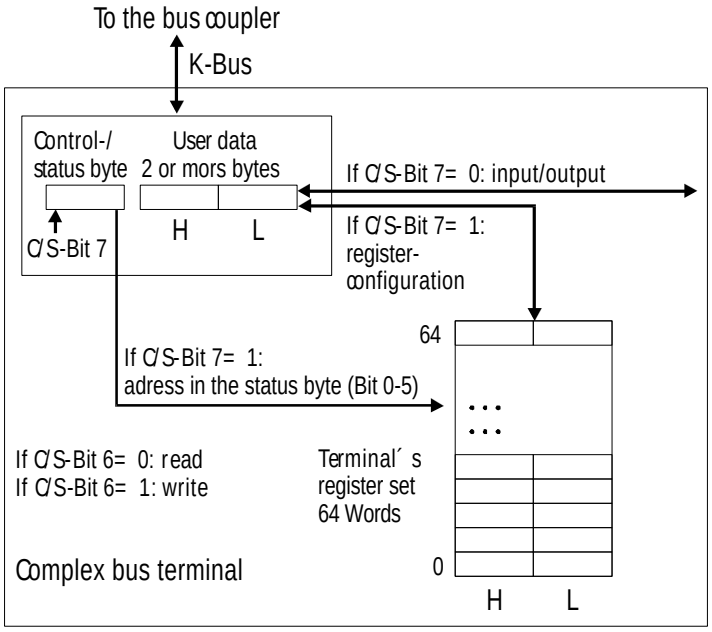
bits 0 to 5: address The address of the register to be addressed is entered in bits 0 to 5 of the control byte.

Control byte in the register mode

MSB

REG=1	W/NR	A5	A4	A3	A2	A1	A0

REG = 0 : Process data transfer
REG = 1 : Access to register structure
W/NR = 0 : Read register
W/NR = 1 : Write register
A5..A0 = Register address
A total of 64 registers can be addressed with the addresses A5...A0.



The control or status byte occupies the lowest address of a logical channel. The corresponding register values are located in the following 2 data bytes. (The BK2000 is an exception to this rule: here, an unused data byte is inserted after the control or status byte, thus setting the register value to a word limit.)

Example

Reading register 8 in the BK2000 with a Kl3022 and the end terminal.

If the following bytes are transferred from the controller to the terminal,

Byte0	Byte1	Byte2	Byte3
0x88	0xXX	0xXX	0xXX

the terminal returns the following type designation (0xBCE corresponds to the unsigned integer 3022)

Byte0	Byte1	Byte2	Byte3
0x88	0x00	0xCE	0x0B

A further example

Writing register 31 in the BK2000 with an intelligent terminal and the end terminal.

If the following bytes user code word) are transferred from the controller to the terminal),

Byte0	Byte1	Byte2	Byte3
0xDF	0xXX	0x12	0x35

the user code word is set and the terminal returns the register address with the bit 7 for register access as the acknowledgement.

Byte0	Byte1	Byte2	Byte3
0x9F	0x00	0x00	0x00

Terminal-specific register description

R32: Feature tegister:
[0x0100]
The feature register defines the terminal's operating mode.

Feature bit no.		Description of the mode
Bit 0	-	No function
Bit 1	0/1	Output format 0: Standard output [0] 1: Alternative output
Bit 2	1	If two counters are active, the CNT_INH bit becomes CNT_SET for the second counter [0].
Bit 3	1	The counter(s) is/are set with a positive edge of the CNT_SET bit in the control byte [0]
Bit 4	1	The internal function for setting output A0 is active [0].
Bit 5	1	The internal function for resetting output A0 is acrive [0].
Bit 6	1	The internal function for setting output A1 is active [0].
Bit 7	1	The internal function for resetting output A1 is active [0].
Bit10 Bit9 Bit8		
	001	32-bit up/down counter [001]. 24-bit if alternatie output format is active.
	010	Standard output: 2 *16-bit up counter Alternative output: counter0 is 8 bits and couner1 is 6 bits wide The counting frequnecy is limited to approximately 5 kHz. Counter 0 (Count input) uses the hardware counter of the controller Counter 1 (VR input) uses the CAP/COM unit of the controller [Pulse width > 100 microsecodns]

Feature bit no.		Description of the mode
	100	32-bit gated counter, VR input is used as gate 24-bit if alternative output format is active VR input low: counter is disabled
	101	32-bit gated counter, VR input is used as gate 24-bit if alternative output is active VR input high: counter is disabled
Bit 11	0/1	Counting direction Up [0] Down
Bit 12	1	Terminal bus access is polled if the bit is set [0]
Bit15,14,13	-	No function

CONTROL byte during process data exchange

The control byte is transferred from the control system to the terminal. It can be used in the register mode (REG = 1) or during process data exchange (REG = 0). The control byte triggers various actions in the counter terminal KL-1501 during process data exchange:

MSB

REG=0	0	CNT_SET	CNT_INH	SET_A1	SET_A0	EN_A1	EN_A0

Bit	Function
CNT_SET	The counter is set to the value that is specified via the process data. Setting of the counter can be edge or level-controlled (see R32).
CNT_INH	The counter is stopped as long as this bit is active. In doing so, the old counter status is retained. If two counters are active, the second counter can be set with this bit.
SET_A1	Sets the second output
SET_A0	Sets the first output
EN_A1	This bit enables the internal function activated by R32.
EN_A0	This bit enables the internal function activated by R32.

STATUS byte During process data exchange

The status byte is transferred from the terminal to the control system. The status byte contains various status bits of the counter terminal KL-1501:

MSB

REG=0	0	SET_ACC	INH_ACC	ST_A1	ST_A0	ST_V/R	ST_CLK

Bit	Function
SET_ACC	The data for setting the counter has been accepted from the terminal.
INH_ACC	The counter is stropped for as long as this bit is set.
ST_A1	The status of output A1 is reflected in this bit.
ST_A0	The status of output A0 is reflected in this bit.
ST_V/R	The status of the V/R input is reflected in this bit.
ST_CLK	The status of the CLOCK input is reflected in this bit.

Setting the outputs A0, A1

The functions for setting the outputs can be armed with the control bits EN_A0, EN_A1. The control bits SET_A0 and SET_A1 are ignored when EN_A0, EN_A1 is set.

Operating modes

V/R counter or gated counter:
An internal function for setting the outputs can activated via the feature register R32.
If the counter reaches the counter sttaus 0x80000000
the output A0 is set (feature bit 5)
or
or is reset (feature bit 6).
If the counter overflows, the output is withdrawn accordingly.
In parallel, output A1 is set with bit 15 (0x8000).

Two counters active:
if the corresponding counter reaches the counter status 0x8000
the output (A1, A0) is set (feature bit 4,6)
or
is reset (feature bit 5,7).
If the counter overflows, the output is withdrawn accordingly.

Example

Feature register = 0x02AC, i.e. two counters are active, the counter is set via the positive edge of the CNT_SET bits and the control bit CNT_INH is responsible for setting the second counter.

A glass is to be filled with 200 ml of beer. In doing so, one pulse corresponds to 0.01 ml, i.e. one glass corresponds to 20000 pulses (0x31E0 = 0x8000-20000)

First counter	Control byte	Status byte	Ouptut data	Output A0	Function
0x0000	0x00	0x00	0x0000	Low	Power on reset
0x0000	0x22	0x00	0x31E0	Low	Counter is set, internal function activated
0x31Ex	0x02	0x28	Don´t care	High	Beer is running
....					
0x8000	0x02	0x00	Don´t care	Low	The first glass is full
...					
0x8000	0x22	0x00	0x31E0	Low	Counter is set, internal function activated
0x31Ex	0x02	0x28	Don´t care	High	Beer is running
....					
0x8000	0x02	0x00	Don´t care	Low	The second glass is full
....					

Annex

As already described in the chapter on terminal configuration, each bus terminal is mapped in the bus coupler. In the standard case, this mapping is done with the default setting in the bus coupler / bus terminal. This default setting can be modified with the TRS Configuration software KS2000 or using Master Configuration (eg ComProfibus). The following tables provide information on how the KL-1501 maps itself in the bus coupler depending on the set parameters.

Standard Format

In the Standard format the KL-1501 is mapped in the bus coupler with 5 bytes input and 5 bytes output data.

Default: CAN CAL, CANopen

DevicNet

		I/O Offset	High Byte	Low Byte
Complete evaluation	= X	3		
MOTOROLA format	= 0	2		D3
Word alignment	= 0	1	D2	D1
		0	D0	CT/ST

Default: Interbus, Profibus

		I/O Offset	High Byte	Low Byte
Complete evaluation	= X	3		
MOTOROLA format	= 1	2		D0
Word alignment	= 0	1	D1	D2
		0	D3	CT/ST

Default: Lightbus

		I/O Offset	High Byte	Low Byte
Complete evaluation	= X	4		
MOTOROLA format	= 0	3	D3	D2
Word alignment	= 1	2	D1	D0
		1	--	CT/ST

		I/O Offset	High Byte	Low Byte
Complete evaluation	= X	4		
MOTOROLA format	= 1	3	D0	D1
Word alignment	= 1	2	D2	D3
		1	--	CT/ST

Alternative Format

In the Alternative format the KL-1501 is mapped in the bus coupler with 4/6 bytes input and 4/6 bytes output data.

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 0	4		
MOTOROLA format	= 0	3		
Word alignment	= 0	2	D2	D1
		1	D0	Cnt-CT/ST

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 0	4		
MOTOROLA format	= 1	3		
Word alignment	= 0	2	D1	D2
		1	Cnt-CT/ST	D0

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 1	4		

MOTOROLA format	= 0	3	D2	D1
Word alignment	= 0	2	--	D0
		1	Cnt-CT/ST	CT/ST

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 1	4		
MOTOROLA format	= 1	3	D1	D2
Word alignment	= 0	2	--	Cnt-CT/ST
		1	D0	CT/ST

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 1	4	D2	D1
MOTOROLA format	= 0	3	--	--
Word alignment	= 1	2	D0	Cnt-CT/ST
		1	--	CT/ST

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 1	4	D1	D2
MOTOROLA format	= 0	3	--	--
Word alignment	= 1	2	Cnt-CT/ST	D0
		1	--	CT/ST

Legend

Complete evaluation: the terminal is mapped with control / status byte.
Motorola format: The Motorola or Intel format can be set.
Word alignment: The terminal is at a word limit in the bus coupler.
CT: Control Byte (appears in the PI of the outputs).
ST: Status Byte (appears in the PI of the inputs).
Cnt-CT: Control Byte in process data exchange
Cnt-ST: Status Byte in process data exchange

Table of the KL-1501 register set

Address	Description	Default	R/W	Storage medium
R0	not used	0x0000	R	
R1	not used	0x0000	R	
R2	not used	0x0000	R	
R3	not used	0x0000	R	
R4	not used	0x0000	R	
R5	not used	0x0000	R	
R6	Diagnostic register – not used	0x0000	R	
R7	Command register - not used	0x0000	R	
R8	Terminal type	1501	R	ROM
R9	Software version number	0x????	R	ROM
R10	Multiplex-shift register	0x0218	R	ROM
R11	Signal channels	0x0128	R	ROM
R12	minimum data length	0x2828	R	ROM
R13	Data structure	0x0000	R	ROM
R14	not used	0x0000	R	
R15	Alignment-register	variable	R/W	RAM
R16	Hardware version number	0x????	R/W	SEEROM
R17	not used	0x0000	R/W	SEEROM
R18	not used	0x0000	R/W	SEEROM
R19	not used	0x0000	R/W	SEEROM
R20	not used	0x0000	R/W	SEEROM
R21	not used	0x0000	R/W	SEEROM
R22	not used	0x0000	R/W	SEEROM
R23	not used	0x0000	R/W	SEEROM
R24	not used	0x0000	R/W	SEEROM
R25	not used	0x0000	R/W	SEEROM
R26	not used	0x0000	R/W	SEEROM
R27	not used	0x0000	R/W	SEEROM
R28	not used	0x0000	R/W	SEEROM
R29	not used	0x0000	R/W	SEEROM
R30	not used	0x0000	R/W	SEEROM
R31	Code word register	variable	R/W	RAM
R32	Feature register	0x0100	R/W	SEEROM
R33	not used	0x0000	R/W	SEEROM
R34	not used	0x0000	R/W	SEEROM
R35	not used	0x0000	R/W	SEEROM
R36	not used	0x0000	R/W	SEEROM
R37	not used	0x0000	R/W	SEEROM
R38	not used	0x0000	R/W	SEEROM
R39	not used	0x0000	R/W	SEEROM
R40	not used	0x0000	R/W	SEEROM
R41	not used	0x0000	R/W	SEEROM
R42	not used	0x0000	R/W	SEEROM
R43	not used	0x0000	R/W	SEEROM
R44	not used	0x0000	R/W	SEEROM
R45	not used	0x0000	R/W	SEEROM
R46	not used	0x0000	R/W	SEEROM
R47	not used	0x0000	R/W	SEEROM