KL-2502

Technical Documentation
2-Channel Puls Width
Output Terminal 24VDC

Please keep for further use !

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"< >" refers to keys on your computer keyboard (e.g. <RETURN>).

Note

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The cover of this document shows the current revision status and the corresponding date. Since each individual page has its own revision status and date in the footer, there may be different revision statuses within the document.

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Revision	Date

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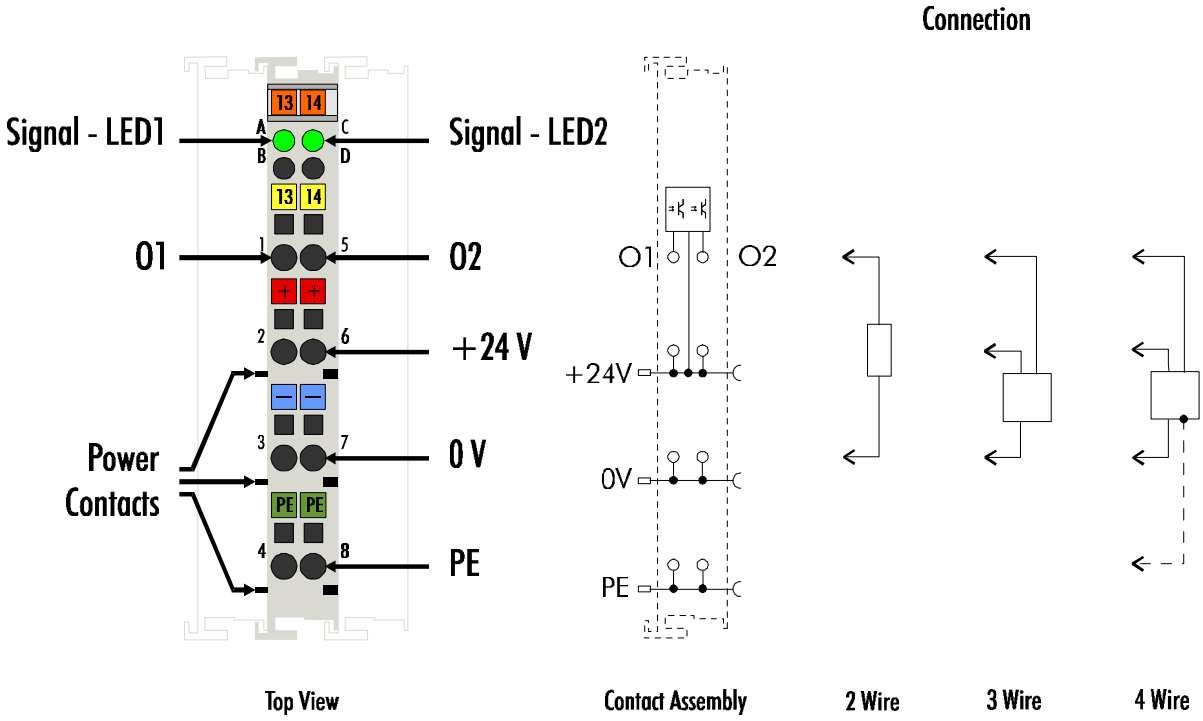
2-Channel Puls Width Output Terminal 24 VDC KL2502



Technical Data	KL2502
Number of outputs	2
Rated load voltage	24 V DC (20 V...29 V)
Load type	ohmic, inductive
Max. output current	0.1 A (short circuit proof)
Fundamental frequency	1 ... 20 kHz, 250 Hz default
Keying ratio	0 ... 100% (T_{ON} > 750 ns, T_{off} > 500 ns)
Resolution	max. 10 bits
Electrical isolation	500 Vrms (T-Bus / field voltage)
Current consumption from T-Bus	18 mA typ.
Current consumption load voltage	10 mA typ.
Bit width in the process image	I/O: 2 x 16 bits data, 2 x 8 bits control/status
Configuration	no address or configuration setting
Weight approximately	50 g
Operating temperature	0°C ... +55°C
Storage temperature	-25°C ... +85°C
Relative humidity	95%, no condensation
Vibration/schock resistance	In accordance with IEC 68-2-6 / IEC 68-2-27
EMC resistance Burst / ESD	In accordance with EN 61000-4-4 / EN 61000-4-2 Limits in accordance with EN 50082-2
Installation position	any
Degree of protection	IP20

Description of functions

The ouput terminal KL2502 modulates the pulse width of a binary signal. The peripheral end of the electronic circuitry is electrically isolated from the internal K bus and therefore also from the field bus. The clock pulse (base frequency) and the pause ratio are adjustable. Via the control system's process image, 16-bit values can be specified for setting.
By default, the terminal KL2502 occupies 6 bytes in the process image. Mapping of the KL2502 is adjustable via the control system or via the bus coupler's configuration interface using the TRS KS2000 configuration software.
Besides operation in the PWM mode, the KL2502 can also be operated in the FM mode (frequency modulation) or in the stepper motor control mode (Frq-Cnt-Pulse mode).
The terminal's default setting is the PWM mode with a base frequency of 250 Hz and a resolution of 10 bits.

LED display

RUN LEDs
On: normal operation
Off: watchdog timer overflow has occurred. If no process data is transferred by the bus coupler for 100 ms, the green LED goes off and the outputs are set to 0% duty cycle.

Process data

Input format: 2's complement representation (-1 corresponds to 0xFFFF)
The duty cycle/period ratio is specified with a maximum resolution of 10 bits.

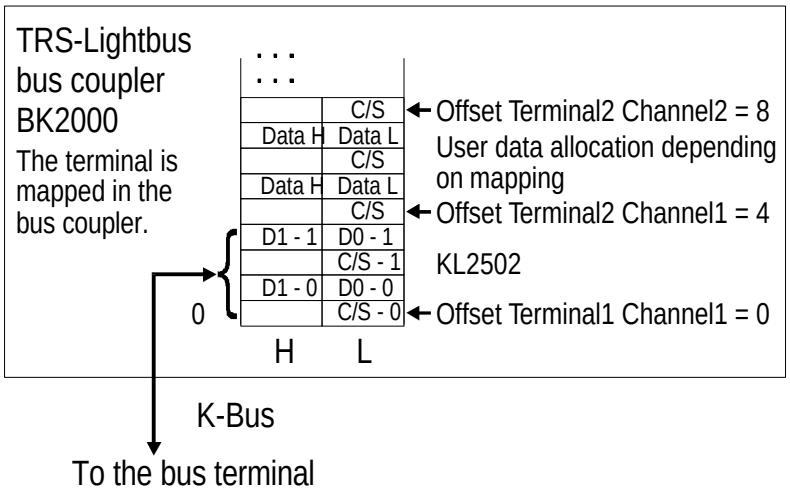
prozess data	output value
0x0000	0% Duty Cycle
0x3FFF	50% Duty Cycle
0x7FFF	100% Duty-Cycle

Terminal configuration

The terminal can be configured and parametrized by way of the internal register structure.
Each terminal channel is mapped in the bus coupler. The terminal's data is mapped differently in the bus coupler's memory depending on the type of the bus coupler and on the set mapping configuration (eg.Motorola / Intel format, word alignment,...). Contrary to the analog input and output terminals, in the case of the KL2502 the control and status byte is always also mapped regardless of the field bus system used.

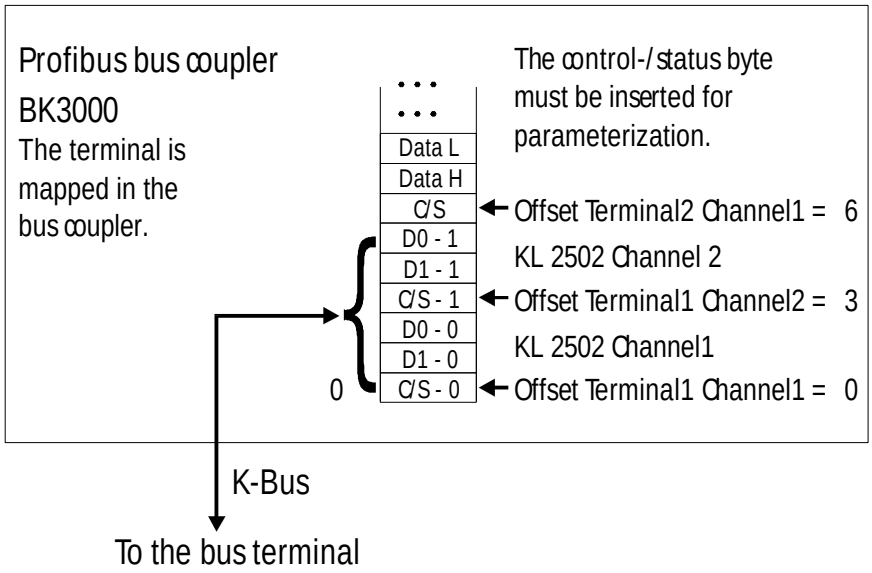
TRS Lightbus Coupler BK2000

In the case of the TRS-Lightbus coupler BK2000, the control /status byte is always mapped besides the data bytes. It is always in the low byte at the offset address of the terminal channel.



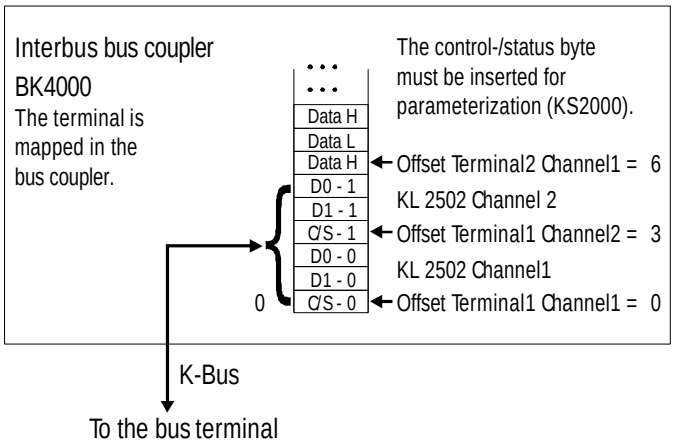
Profibus Coupler BK3000

In the case of the Profibus coupler BK3000, by default the KL2502 is mapped with 6 bytes of input data and 6 bytes of output data (3 bytes per channel). Therefore, 2 bytes of user information data and 1 control/status byte are mapped for each channel.



Interbus Coupler BK4000

By default, the Interbus coupler BK4000 maps the KL2502 with 6 bytes of input and 6 bytes of output data. Parametrization via the field bus is not possible.The KS2000 software is needed for configuration if it is intended to use the control / status byte.



Other bus couplers and further information

You will find further information on the mapping configuration of bus couplers in the annex of the respective bus coupler manual under the heading of "Configuration of Masters".

Reference

The annex contains an overview of the possible mapping configurations depending on the adjustable parameters.

Parametrization with the KS2000 software

Parametrization operations can be carried out independently of the field bus system using the TRS KS2000 configuration software via the serial configuration interface in the bus coupler.

KL2502 register communication

General register description

Complex terminals that possess a processor are capable of bidirectionally exchanging data with the higher-level control system. Below, these terminals are referred to as intelligent bus terminals. They include the analog inputs (0-10V, -10-10V, 0-20mA, 4-20mA), the analog outputs (0-10V, -10-10V, 0-20mA, 4-20mA), serial interface terminals (RS485, RS232, TTY, data transfer terminals), counter terminals,the encoder interface, the SSI interface, the PWM terminal and all other parametrizable terminals.

Internally, all intelligent terminals possess a data structure that is identical in terms of its essential characteristics. This data area is organized in words and embraces 64 memory locations. The essential data and parameters of the terminal can be read and adjusted by way of this structure. Function calls with corresponding parameters are also possible. Each logical channel of an intelligent terminal has such a structure (therefore, 4-channel analog terminals have 4 register sets).

This structure is broken down into the following areas:
(You will find a list of all registers at the end of this documentation).

Area	Address
Process variables	0-7
Type registers	8-15
Manufacturer parameters	16-31
User parameters	32-47
Extended user area	48-63

Process variables

R0 - R7 Registers in the terminal's internal RAM

The process variables can be used in addition to the actual process image and their functions are specific to the terminal.

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R0 - R5: These registers have a function that depends on the terminal type.

R6: Diagnostic register

The diagnostic register may contain additional diagnostic information. In the case of serial interface terminals, for example, parity errors that have occurred during data transfer are indicated.

R7: Command register

High-Byte_Write = function parameter
Low-Byte _Write = function number
High-Byte _Read = function result
Low-Byte_ Read = function number

Type registers

R8 - R15 Registers in the terminal's internal ROM

The type and system parameters are programmed permanently by the manufacturer and can only be read by the user, but cannot be modified.

R8: Terminal type

The terminal type in register R8 is needed to identify the terminal.

R9: Software version X.y

The software version can be read as an ASCII character string.

R10: Data length

R10 contains the number of multiplexed shift registers and their length in bits. The bus coupler sees this structure.

R11: Signal channels

In comparison with R10, the number of logically existing channels is located here. For example, one physically existing shift register may consist of several signal channels.

R12: Minimum data length

The respective byte contains the minimum data length of a channel to be transferred. The status byte is omitted if the MSB is set.

R13: Data type register

Data type register	
0x00	Terminal without valid data type
0x01	Byte array
0x02	1 byte n bytes structure
0x03	Word array
0x04	1 byte n words structure
0x05	Double word array
0x06	1 byte n double words structure
0x07	1 byte 1 double word structure
0x08	1 byte 1 double word structure

Data type register	
0x11	Byte array with a variable logical channel length
0x12	1 byte n bytes structure with a variable logical channel length (eg 60xx)
0x13	Word array with a variable logical channel length
0x14	1 byte n words structure with a variable logical channel length.
0x15	Double word array with a variable logical channel length
0x16	1 byte n double words structure with a variable logical channel length

R14: not used

R15: Alignment bits (RAM)

The analog terminal is set to a byte limit in the terminal bus with the alignment bits.

Manufacturer Parameters

R16 - R30 is the area of the "Manufacturer Parameters" (SEEROM)

The manufacturer parameters are specific to each terminal type. They are programmed by the manufacturer, but can also be modified from the control system. The manufacturer parameters are stored permanently in a serial EEPROM in the terminal and are therefore not destroyed by power failures.
These registers can only be modified after setting a code word in R31.

User Parameters

R31 R47 " Application Parameters" area (SEEROM)

The application parameters are specific to each terminal type. They can be modified by the programmer. The application parameters are stored permanently in an serial EEPROM in the terminal and cannot be destroyed by power failures. From software version 2.A, the user area is write-protected by way of a code word.

R31: Code word register in the RAM

The code word 0x1235 must be entered here to enable modification of parameters in the user area. Write protection is set if a different value is entered in this register. When write protection is inactive, the code word is returned during reading of the register. The register contains the value zero when write protection is active.

R32: Feature register

This register defines the operating modes of the terminal. For example, a user-specific scaling can be activated for the analog I/O`s.

R33 - R47

Registers that depend on the terminal type

Extended application area

R47 - R63

These registers have not yet been implemented.

Register access via process data transfer.

bit 7=1: register mode

When bit 7 of the control byte is set, the first two bytes of the user data are not used for process data transfer, but are written into or read out of the terminal’s register set.

bit 6=0: read
bit 6=1: write

In bit 6 of the control byte, you define whether a register is to be read or written. When bit 6 is not set, a register is read without modification. The value can be taken from the input process image.
When bit 6 is set, the user data is written into a register. The operation is concluded as soon as the status byte in the input process image has assumed the same value as the control byte in the output process image.

Bits 0 to 5: address

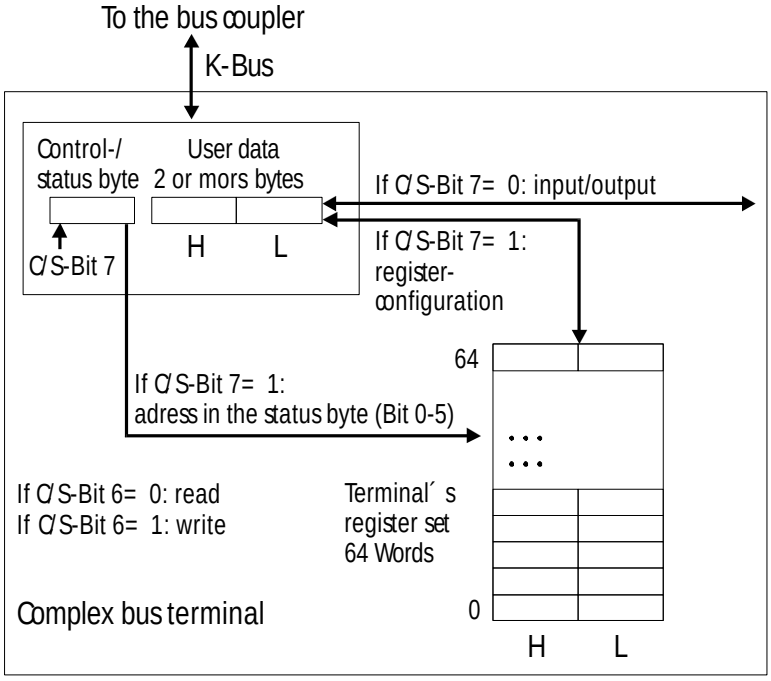
The address of the register to be addressed is entered in bits 0 to 5 of the control byte.

Control byte in the register mode

MSB

REG=1	W/NR	A5	A4	A3	A2	A1	A0

REG = 0 : Process data transfer
REG = 1 : Access to register structure
W/NR = 0 : Read register
W/NR = 1 : Write register
A5..A0 = Register address
A total of 64 registers can be addressed with the addresses A5...A0.



The control or status byte occupies the lowest address of a logical channel. The corresponding register values are located in the following 2 data bytes (the BK2000 is an exception to this rule: here, an unused data byte is inserted after the control or status byte, thus setting the register value to a word limit).

Example

Reading register 8 in the BK2000 with a Kl3022 and the end terminal.

If the following bytes are transferred from the controller to the the terminal

Byte0	Byte1	Byte2	Byte3
0x88	0xXX	0xXX	0xXX

the terminal returns the following tyte designation (0xBCE corresponds to the unsigned integer 3022)

Byte0	Byte1	Byte2	Byte3
0x88	0x00	0xCE	0x0B

A further example

Writing register 31 in BK2000 with an intelligent terminal and the end terminal.

If the following bytes (user code word) are transferred from the controller to the terminal,

Byte0	Byte1	Byte2	Byte3
0xDF	0xXX	0x12	0x35

the user code word is set and the terminal returns the register address with the bit 7 for register access as the acknowledgement.

Byte0	Byte1	Byte2	Byte3
0x9F	0x00	0x00	0x00

Terminal-specific register description

Process variables

R0,R1: no function

R2: period
In the PWM mode, the period for current operation can be specified here. Following a power on reset, the period is taken from R35.

PWMH mode, Cnt-Cnt PWM mode:

1 digit corresponds to one 1 microsecond here
e.g.: 250 Hz => 4000 µs = 0xFA0
4 KHz => 250 µs = 0xFA

PWML mode, Frq-Cnt PWM mode, Frq-Cnt pulse mode:

1 digit corresponds to 8 microseconds
e.g.: 2 Hz => 500 ms = 0xF424
200Hz => 5 ms = 0x271

R3: base frequency
In the PWM mode, the base frequency can be specified here. [R/W]

1 digit corresponds to 1 Hz

R5: PWM raw vale
The value of the processor's PWM unit is stored in this register. The maximum resolution for a given frequency can be computed with this value.

R6: diagnostic register
Not used

Manufacturer parameters

R19: manufacturer offset B_h
16-bit signed integer
Linear equation: Y = A_h X + B_h
This register contains the offset of the manufacturer's linear equation. The linear equation is activated via R32.

R20: manufacturer scaling A_h
16-bit unsigned integer * 2^-8
This register cotnains the scaling value of the manufacturer's linear equation. The linear equation is activated via R32.

1 corresponds to the register value 0x0100

Application parameters

R32: feature register:
[0x0000]
The feature register defines the terminal's operating mode.

Feature bit No.		Description of the mode	
Bit 0	1	User scaling active [0]	
Bit 1	1	Manufacturer scaling active [0]	
Bit 2	1	Watchdog timer active. If the terminal does not receive any data for 100 ms, the PWM signal is set to 0% duty cycle. [0]	
Bit 12-3	-	Not used	
Bit 15,14,13		Mode	Value range
	000	PWMH mode [000]	250 Hz to 20 kHz
	001	PWML mode	2 Hz to 250 Hz
	011	Frq-Cnt PWM mode	2 Hz to 2 kHz
	101	Frq-Cnt pulse mode	2 Hz to 2 kHz
	111	Cnt-Cnt PWM mode	250 Hz to 8 kHz

R33: user offset B_w
16-bit signed integer

Linear equation: Y = A_w X + B_w

This register cotnains the offset of the user linear equation. The linear equation is activated via R32.

R34: User scaling A_w
16-bit signed Integer * 2^-8

This register contains the scaling factor of the user linear equation. The linear equation is activated via R32.

R35: period for PWM mode
[0x0FA0]
Subsequent to a restart of the processor, the period of R35 is entered in R2.
During operation, this can be modified via R2 or R3.
Input is as described in R2.

R36: duty cycle
[0x4000]
The ratio of the duty cycle to the period in the Frq-Cnt-PWM mode and in the Cnt-Cnt-PWM mode is defined by this register.

0x2000 corresponds to 25% duty cycle
0x4000 corresponds to 50% duty cycle

R37: pulse duration for teh Frq-Cnt pulse mode
[0x0005]
The pulse duration in the Frq-Cnt pulse mode is entered in this register.

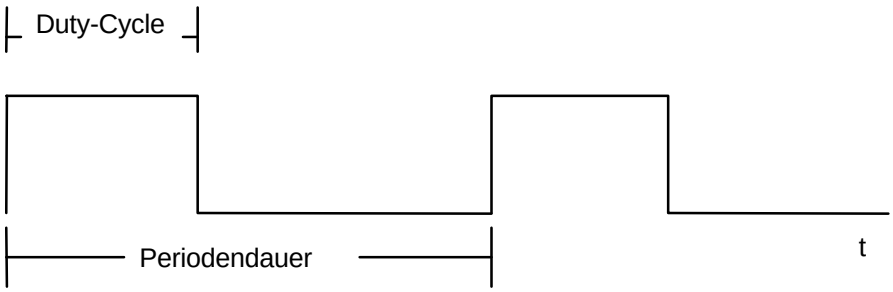
1 digit corresponds to 8 microseconds.

Operating modes

The operating mode of the terminal is set via the feature register R32.

PWM mode

In the PWMx mode, two channels can be operated. Attention must be paid to the fact that the operating mode and the period are identical for both channels.



PWMH

In the PWM mode, the ratio of the duty cycle to the period is specifed via the process data.
In doing so, 100% duty cycle corresponds to the process data item 0x7FFF. During operation, the period can be specified via the register R2. This is loaded out of R35 (SEEROM) after a system start and is entered in R2.
The frequency range is from 245 Hz to 20 kHz (0xFA0 in R2 correpsonds to 250 Hz) with a resolution of 10 bits at 245 Hz, 976 Hz and 3.9 kHz.

PWML

In the PWM mode, the ratio of the duty cycle to the period is specified via the process data.
In doing so, 100% duty cycle corresponds to the process data item 0x7FFF (32767). During operation, the period can be specified via the register R2. After a system start, this is loaded out of R35 (SEEROM) and is entered in R2.
The frequency range is from 2 Hz to 250 Hz (250 Hz corresponds to 0x1F4 in R2).

Frq-Cnt-PWM mode

Via the process output data of the control system, the frequency is specified as 2 Hz per digit. The number of periods output by the terminal is returned to the control system as process input data. In this operating mode, the counting direction is defined by the sign of the output data. Here, 2 Hz corresponds to the value 0x0001 and -2Hz corresponds to the value 0xFFFF (signed integer). The frequency ranges from 2 Hz to 2 kHz. The pulses are output in channel 0 and the counting direction is output in channel 1. "Down" corresponds to the GND level and "up" corresponds to the Vcc (24V) level.

The counter is set to the value of the output data with a rising edge of the control bits0 (control byte in the process data mode, i.e. bit7 = 0).

The pulse width ratio is defined via R36.

Frq-Cnt pulse mode

The frequency is specified as 2 Hz per digit via the process output data of the control system. The number of pulses output by the terminal is returned to the control system as process input data. In this operating mode, the counting direction is defined via the sign of the output data. Here, 2 Hz corresponds to the value 0x0001 and -2Hz corrresponds to the value 0xFFFF (signed integer). The pulses are output in channel0 and the counting direction is output in channel1. "Down" corresponds to the GND level and "up" corresponds to the Vcc level.
The frequency range is from 2 Hz to 2 KHz.

The counter is set to the value of the output data with a rising edge of the control bit0 (control byte in the process data mode, i.e. bit7 = 0)..

The fixed pulse width for all frequencies is defined via R37.

Cnt-Cnt-PWM mode

The number of pulses is specified via the process output data. The number of output periods is returned to the control system as process input data. At the same time, the pulse width ratio is defined via R36 and the period is defined via R35. Ouptut is started with a positive edge of control bit 0. Output can be retriggered with each further edge. The pulses are output in channel 0, Channel1 can be started via conrol bit 2. Acceptance and simultaneous starting of pulse output is returned as status information to the control system in status bit0. Status bit1 remains for as long as output is active and status bit 2 returns the status of channel 1.

Annex

As already described in the chapter on terminal configuration, each bus terminal is mapped in the bus coupler. In the standard case, this mapping is done with the default setting in the bus coupler/bus terminal. This default setting can be modified with the TRS KS2000 configuration software or using master configuration software (e.g. ComProfibus). The following tables provide information on how the KL2502 maps itself in the bus coupler depending on the set parameters.

Mapping in the bus coupler

The KL2502 is mapped in the bus coupler with 6 bytes input and 6 bytes output data.

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 1	3		
MOTOROLA format	= 0	2	D1 - 1	D0 - 1
Word alignment	= 0	1	CT/ST - 1	D1 - 0
		0	D0 - 0	CT/ST - 0

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 1	3		
MOTOROLA format	= 1	2	D0 - 1	D1 - 1
Word alignment	= 0	1	CT/ST - 1	D0 - 0
		0	D1 - 0	CT/ST - 0

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 1	3	D1 - 1	D0 - 1
MOTOROLA format	= 0	2		CT/ST - 1
Word alignment	= 1	1	D1 - 0	D0 - 0
		0		CT/ST - 0

		I/O Offset	High Byte	Low Byte
Complete evaluation	= 1	3	D0 - 1	D1 - 1
MOTOROLA format	= 1	2		CT/ST - 1
Word alignment	= 1	1	D0 - 0	D1 - 0
		0		CT/ST - 0

Legend

Complete evaluation: the terminal is mapped with control / status byte.
Motorola format: the Motorola or Intel format can be set.
Word alignment: the terminal is at a word limit in the bus coupler.
CT: Control- Byte (appears in the PI of the outputs).
ST: Status- Byte (appears in the PI of the inputs).
D0 - 0 : D0 = Data-Low-Byte, 0 = channel 1
D1 – 1 : D1 = Data-High-Byte, 1 = channel 2

Table of the KL2502 register set

Address	Description	Default	R/ W	Storage medium
R0	not used	0x0000	R	
R1	not used	0x0000	R	
R2	Period	variable	R	RAM
R3	Fundamental frequency	variable	R	RAM
R4	not used	0x0000	R	
R5	Raw PWM value	variable	R	RAM
R6	Diagnostic register - not used	0x0000	R	
R7	Command register - not used	0x0000	R	
R8	Terminal type	2502	R	ROM
R9	Software version number	0x????	R	ROM
R10	Multiplex shift register	0x0218	R	ROM
R11	Signal channels	0x0218	R	ROM
R12	Minimum data length	0x1818	R	ROM
R13	Data structure	0x0000	R	ROM
R14	not used	0x0000	R	
R15	Alignment register	variable	R/W	RAM
R16	Hardware version number	0x????	R/W	SEEROM
R17	not used	specific	R/W	SEEROM
R18	not used	specific	R/W	SEEROM
R19	Manufacturer scaling: offset	0x0000	R/W	SEEROM
R20	Manufacturer scaling: gain	0x0020	R/W	SEEROM
R21	not used	0x0000	R/W	SEEROM
R22	not used	0x0000	R/W	SEEROM
R23	not used	0x0000	R/W	SEEROM
R24	not used	0x0000	R/W	SEEROM
R25	not used	0x0000	R/W	SEEROM
R26	not used	0x0000	R/W	SEEROM
R27	not used	0x0000	R/W	SEEROM
R28	not used	0x0000	R/W	SEEROM
R29	not used	0x0000	R/W	SEEROM
R30	not used	0x0000	R/W	SEEROM
R31	Code word register	variable	R/W	RAM
R32	Feature register	0x0000	R/W	SEEROM
R33	User offset	0x0000	R/W	SEEROM
R34	User gain	0x0100	R/W	SEEROM
R35	Period PWM	0x0000	R/W	SEEROM
R36	Duty-Cycle	0x0000	R/W	SEEROM
R37	Pulse-Radiation	0x0000	R/W	SEEROM
R38	not used	0x0000	R/W	SEEROM
R39	not used	0x0000	R/W	SEEROM
R40	not used	0x0000	R/W	SEEROM
R41	not used	0x0000	R/W	SEEROM
R42	not used	0x0000	R/W	SEEROM
R43	not used	0x0000	R/W	SEEROM
R44	not used	0x0000	R/W	SEEROM
R45	not used	0x0000	R/W	SEEROM
R46	not used	0x0000	R/W	SEEROM
R47	not used	0x0000	R/W	SEEROM