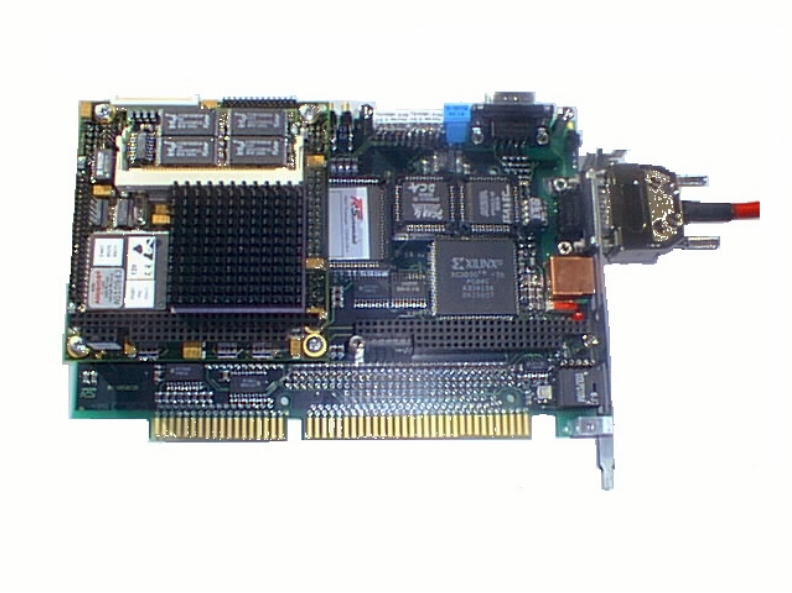
Slot-PLC SPC-210



PLC - for ISA bus, integrable in every PC

SPC-100	**Slot-PC without field bus interface**
SPC-200	**Slot-PC with TRS Lightbus**
SPC-210	**Slot-PC with TRS Lightbus**
SPC-300	**Slot-PC with Profibus-DP**
SPC-400	**Slot-PC with Interbus-S**
SPC-410	**Slot-PC with Interbus-S**
SPC-500	**Slot-PC with CAN - CAL**
SPC-510	**Slot-PC with CAN - Open**
SPC-520	**Slot-PC with CAN DeviceNet**

Software Simatic S5 (CPU 945) compatible, serial protocol AS511

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Printing

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Fonts

Italics and **bold** type are used for the title of a document or to emphasize text passages.

Passages written in Courier show text which is visible on the display as well as software menu selections.

"< >" refers to keys on your computer keyboard (e.g. <RETURN>).

Note

Text following the "NOTE" symbol describes important features of the respective product.

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Revision History

Note:
The cover of this document shows the current revision status and the corresponding date. Since each individual page has its own revision status and date in the footer, there may be different revision statuses within the document.

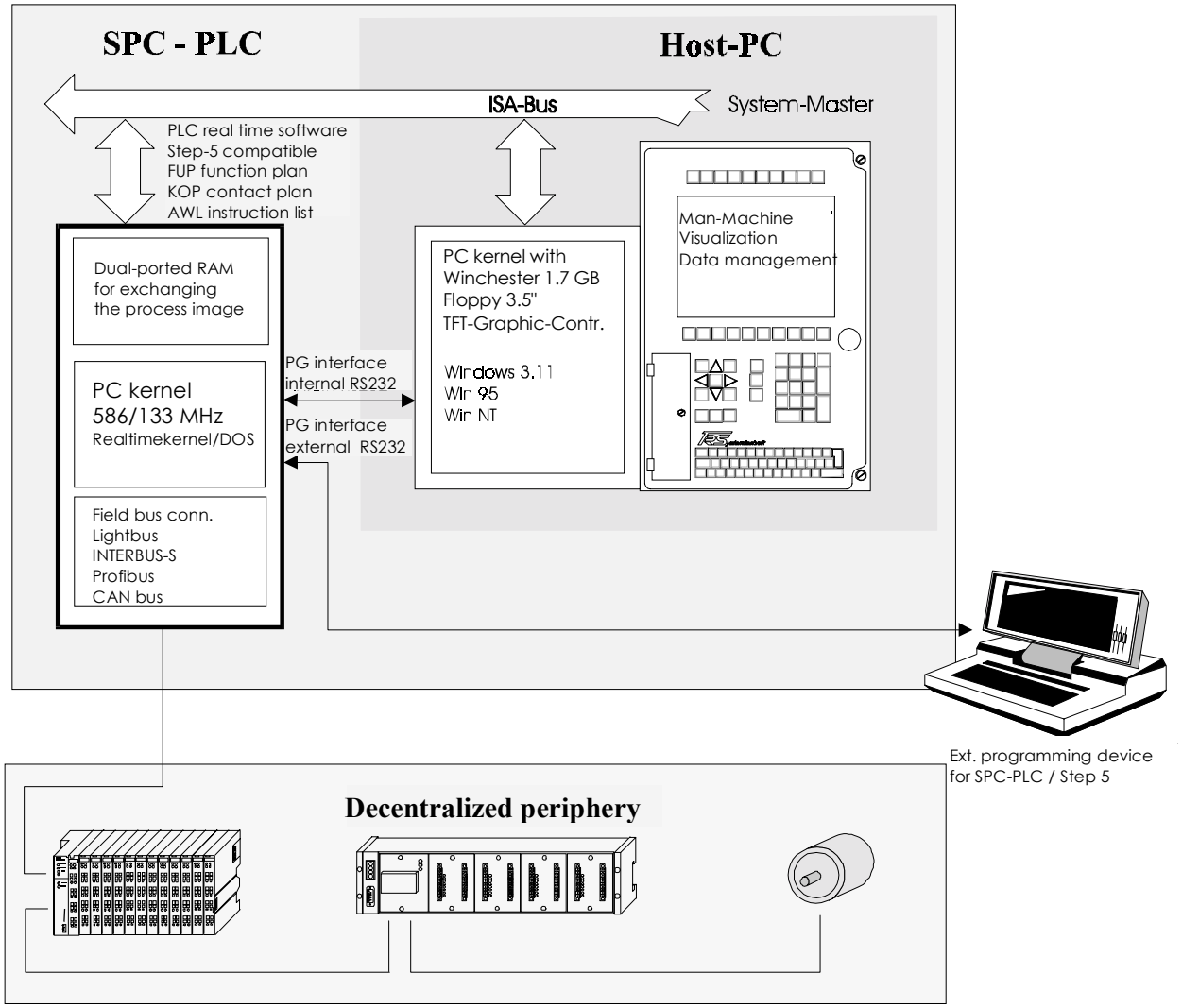
Document created: 04.12.1998

Revision	Date
Supplementations: programming of DB1, example DB1, error table functional module, communication via DPRAM; hardware identification replaced by component identification New: transfer of 5 data blocks in a SPS-cycle	18.01.1999
Appendix: Various installation possibilities of a SPC	27.10.1999

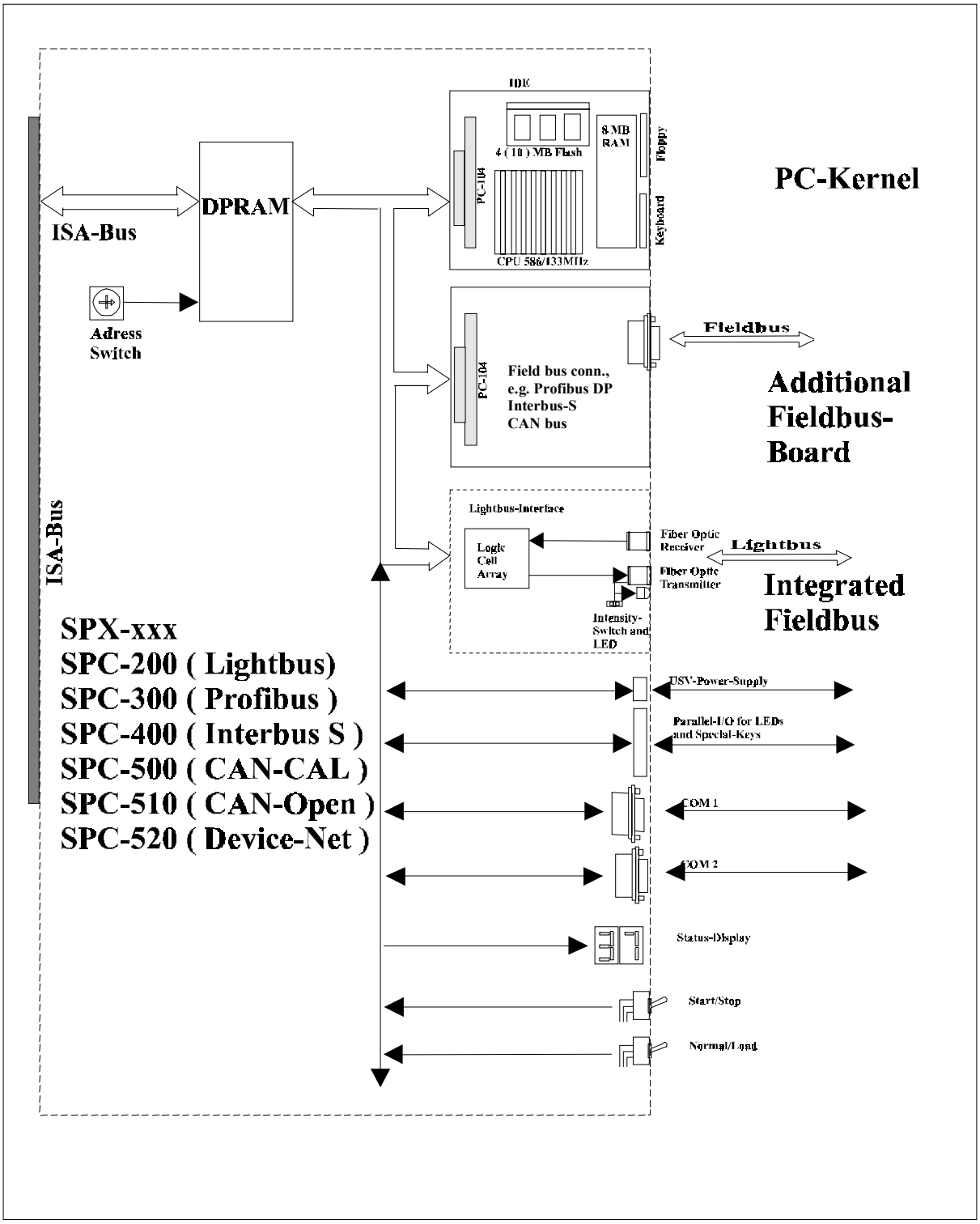
TABLE OF CONTENTS

1 General information

- The SPC component is a PLC (Programmable Logical Control), which can be integrated in any PC.
- The PLC communicates with the higer-level host PC via a dual-ported RAM. In this dual-ported RAM, the process image is provided.
- One of the two serial interfaces of the SPC is used for programming the PLC. This offers the possibility to program the PLC not only with the host PC, but also by means of an external laptop or a Siemens programmer. The AS511 (optionally an IBH Softec protocol as well) is used as a protocol at the serial interface.
- The PLC disposes of the capacity range of a SIEMENS 945 CPU, regarding the command set.



2 Block circuit diagram



The SPC consists of several components

A base board containing the following components.

a) 8 KB dual-ported RAM for communication with the ISA bus
b) Two PC-104 slots
c) Plug for two serial interfaces
d) Integrated lightbus connection
e) Integrated CAN bus connection
f) Interface to an NPS power supply unit
g) Parallel interface for offset switches and display
h) 7-segment displays for displaying the status
i) Switch for Run/Stop
j) Switch for normal/special operation
k) Key for Reset
l) Key for Load
m) 4 MB FLASH EPROM
n) Optionally up to 1 MB SRAM

A PC (IBM-compatible) which is plugged in either of the two PC-104 slots and which contains the following components.

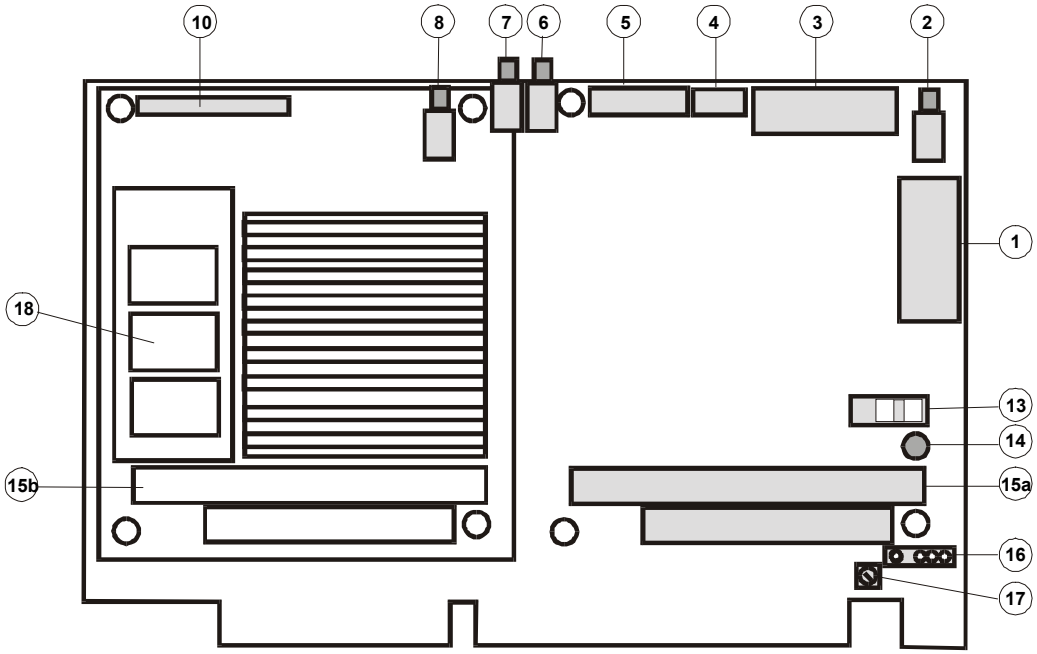
a) CPU 586 / 133 MHz
b) 4 MB RAM (extensible)
c) 800 KB Flash Eprom as drive "C:"
d) 4 MB Flash Eprom as drive "D:" (extensible)
e) Two serial interfaces COM 1 and COM 2
f) One parallel interface
g) Connection for floppy drive
h) Connection for keyboard

A second PC-104 slot which can be used for expansion boards.

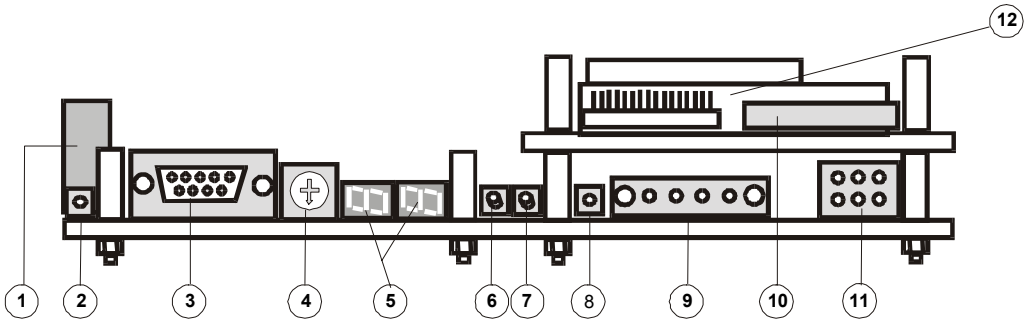
a) Profibus DP connection
b) Interbus-S connection
c) CAN bus connection (unless the integrated one is used)
d) Any other boards such as VGA controller, etc.

3 Views of the SPC

Top view:



Front view:



1	Serial interface COM 1
2	Reset key
3	Serial interface COM 2
4	Address setting segment address dual-ported RAM
5	Status display
6	RUN/STOP PLC switch
7	PLC mode / Interlink mode switch
8	Reload Flash key
9	Plug for external voltage supply
10	Connection for floppy drive
11	Interface NPS (Non-interrupted power supply)
12	PC kernel based on PC-104 , CPU 586/133MHz with Flash
13	Intensity switch for lightbus
14	Intensity display
15a	PC-104 plug for field bus connections such as Profibus DP, Interbus-S, CAN bus
15b	PC-104 plug for PC kernel
16	Connection for ext. keyboard
17	Balancing of transmitting power for lightbus
18	Connection for hard disk or flash disk

1 **Serial interface COM 1**

Either laptop or Siemens PG.
In the interlink mode, COM 1 can be used for updating the firmware or for modifying the initialization files.

2 **Reset key**

With this key, the PLC-CPU can be reset.

3 **Serial interface COM 2**

In the PLC mode, an external programmer can also be connected to COM 2. Either laptop or Siemens PG.
In the interlink mode, COM 2 can also be used for updating the firmware or for modifying the initialization files.

4 **Address setting segment address dual-ported RAM**

The basic address of the dual-ported RAM is set here. The size of the dual-ported RAM is 8 KB.

Switch position	Segment address
0	0D000H
1	0D200H
2	0D400H
3	0D600H
4	0D800H
5	0DA00H
6	0DC00H
7	0DE00H

Default setting

5 **Status display**

The status display is a 2-digit 7-segment display indicating the status of the PLC or error messages

Display	Signification
1	PLC = RUN
0	PLC = STOP

In case of error messages, the display flashes. The error messages are explained in Chapter 5 Error messages.

6 **RUN/STOP PLC switch**

This key starts or stops the PLC.

Position	Signification
Left	PLC = RUN
Right	PLC = STOP

Position left signifies that the switch points away from the base board.
Position right signifies that the switch points towards the base board.

7 **PLC mode / Interlink mode switch**

This switch has several functions. On switching on the SPC component, the position of this switch decides whether the component starts in PLC mode or in interlink mode.

Position	Signification
Left	PLC mode
Right	Interlink mode

In the interlink mode, either the firmware can be updated or the initialization files can be modified.

In the PLC mode, this switch allows to store the current PLC program from the RAM in the Flash Eprom or in the SRAM. During storage, the flashing value "80" is shown in the status display. After completion of storage, the status display indicates an "0" = current PLC Stop.

Position	Signification
Left	PLC mode
Right	Store PLC program

In order to switch over between PLC mode and interlink mode or vice versa, first press the RESET key, then change the switch position.

ATTENTION: If switching is accidentally performed in the PLC mode first, wait until storage is completed before pressing the RESET key (status display = "0"), since the **PLC** program may be destroyed during storage.

8 **Reload Flash key**

When using the TRS NPS power supply unit, the Reload Flash key allows to reload the PLC program from the flash disk if it should have got lost in the SRAM.

9 **Plug for external voltage supply**

If the SPC is operated outside a PC, or if a power supply unit board with TRS NPS power supply unit is used, the supply voltage is connected via this plug.

10 **Connection for floppy drive**

Using a special cable, a floppy drive can be connected to the PC kernel.

11 **Interface NPS (Non-interrupted Power Supply)**

A flash or a battery-buffered SRAM serves for storing remanent flags and data blocks. The power supply unit generates a signal indicating to the PC kernel that the power supply has broken down. Now the CPU stores in the flash or in the SRAM and then switches off the NPS supply.

12 **PC kernel based on PC-104, CPU 586/133MHz**

13 **Intensity switch for lightbus**

The intensity of the OWG transmitter can be modified via the switch. If the LED display Intensity is flasing, transmission is performed with high intensity. When using OWG cables shorter than 15m, low intensity should be activated. In this case, the LED display Intensity is dark.

14 **Display Intensity**

LED ON	**High intensity for cable lengths > 10 m**
LED OFF	**Lowered intensity for cable lengths < 10 m**

15a **PC-104 plug for expansion boards**

Any PC-104 modules can be plugged on this plug. Field bus connections such as profibus DP, interbus-S or CAN bus are plugged here.

15b **PC-104 plug for PC kernel**

16 **Connection for ext. Keyboard**

An ext. keyboard can be connected to the PC kernel. Thus, together with a VGA board, a PC kernel can become a complete PC.

17 **Balancing of transmitting power for lightbus**

The transmitting power (intensity) of the lightbus interface is balanced at the factory.

18 **Connection for hard disk or flash disk**

Using a special cable, a hard disk can be connected to the PC kernel.
In delivery state, a flash disk is attached to this connection.

4 Starting the SPC with Lightbus

1. Make sure that the address range D000H up to D1FFH in your PC is free (default setting on delivery). If this address range is already occupied, choose another address range using the switch for address setting of the segment address.

2. Plug the SPC in a vacant ISA slot in your PC.

3. Now switch on your PC. If the PLC mode / interlink mode switch is in PLC mode position, a flashing error message is shown in the status display after booting the SPC. This error message only indicates that no PLC program has been transmitted to the SPC yet.

4. Now install the system configurator for the lightbus on your host PC or an external programmer you can find on the enclosed CD. For the SPC, configuration is performed via the serial interface.

5. Now the interbus master component must be parameterized using the system configurator. This signifies that the master component is informed about the users connected to the interbus and about the I/O addresses where they have to store their data. The system configurator to be found on the host PC or an external programmer must be connected with the lightbus master component via a zero modem cable. The parameterized interface is located on the slot plate which is connected with the SPC by the two flat conductor cables. The lower sub D plug is for parametering, the upper sub D plug is for the lightbus.

6. When the parameterization of the lightbus master component is completed, connect COM 1 of the SPC with your host PC or with the external programmer, thus you can start programming the PLC program. As default, the SPC is adjusted to the Siemens AS-511 serial protocol.

7. Now you can start programming the PLC program. If you use the programming software "S5W" by IBH-Softec for programming, adjust in the menu "Project" as interface, COM 1 or COM 2, and as appliance Siemens PLC (AS511).
   If you use a Siemens programmer or another programming software, make sure that a corresponding setting is performed.

8. A fixed programmed status block (default FB 10) is available in the lightbus PLC.
   If you are not agreed with the STATUS FB number = 10, you can change this as follows:

   The file "LWLDRV10.INI" is located in the path "PLC43" on drive "D". In this file the number of the status functional block is defined.
   If you wish to change it now, create an interlink connection to your host PC or a programmer. This is necessary as otherwise an access to the drives of the SPC is not possible. The interlink connection is performed via the serial interface. Thus you can use the serial cable of the programmer (zero modem cable).

   To create an interlink connection, insert the following line into the file "CONFIG.SYS" on your host PC and reboot the latter:

   DEVICE=C:\DOS\INTERLNK.EXE /COM:1 /DRIVES:4 /NOPRINTER /NOSCAN

   If you use COM 2 on your host PC, insert /COM:2.

   Now switch the SPC to the interlink mode by pressing the Reset key and then turning the "PLC mode / Interlink mode" to the right into the position "Interlink mode". The SPC reboots and provides its drives to the host PC via interlink. Now you can edit the file LWLDRV10.INI with an editor. Regarding the signification the entries, refer to the chapter "Configuration of the real time PLC". After completion of the modifications, switch back the SPC to the PLC mode by pressing the Reset key and then turning the "PLC mode / Interlink mode" switch to the left into the position "PLC mode". The SPC then reboots.

9. Now start the programming interface, e.g. S5W by IBHSoftec. Click on the icon PLC module directory. The lower status line indicates the serial transmission of the OBs, PBs, FBs etc.

10. Now start your PLC program by turning the RUN / STOP switch to the right (Stop PLC) and back again to the left (RUN-PLC). If the PLC program is perfect, the status display indicates with a 1 that the PLC runs. If the status display indicates an 0, the PLC is in STOP.

11. Now the PLC program is stored in the RAM memory of the SPC. In order that the program will still be available after connecting and disconnecting the supply voltage of the SPC, you have to store it in the flash of the SPC turning the switch "PLC mode / Interlink mode" to the right into the mode "PLC program store". Now the SPC indicates by a flashing 80 in the status display that the data will be stored. The end of storage is displayed by an 0 in the status display which no longer flashes. During storage, the PLC is set to stop and must be restarted with the RUN / STOP switch afterwards.

5 Programming of the real time PLC for the Lightbus

5.1 Programming of the data block DB 1

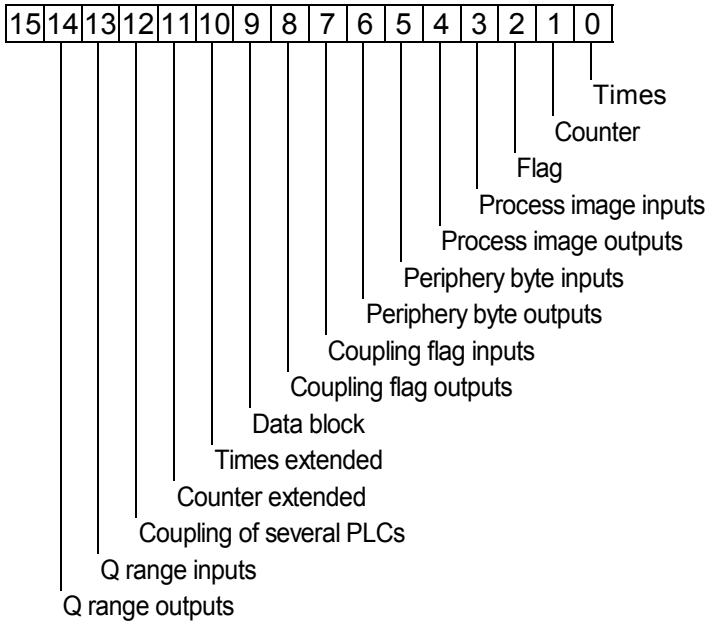
The data block DB1 is used for parameterizing the SPC from the PLC program. In contrast to the file LWLDRV10.INI where parameters are firmly set, DB 1 allows to modify parameters during PLC programming as well. Make sure that the PLC program is restarted when values are modified in the DB1, since the modified values are only activated after a STOP/RUN.
The DB1 is divided in 8 data blocks which are explained below. The first data word of the data blocks 2 - 8 contains a detection CODE which determines the function that is executed by this data block. The further data words of a data block are parameters of the individual functions. The sequence of the data blocks 2 – 8 is optional. Data block 1 contains a header identifying the DB1 as parameterization DB. The end of the DB1 is defined by the end identification. If the data block DB1 is not programmed, or if there is no header, none of the functions for the blocks 2 – 8 is executed. If individual blocks are not defined, only the functions of these blocks are not executed.
If the DB1 is not available, if faulty entries have been found in the DB1, or if there is no end identification, an error message is generated which is output in the status functional module in the parameter **ERN.**

Block 1: Header:
The first 3 data words of the DB1 contain the ASCII code for the string "MASK01"
KH = 4D41 "MA"
KH = 534B "SK"
KH = 3031 "01"
If there is no header, the DB1 is not accepted as parameterization DB, and none of the following blocks has a function.

Block 2: Code CE00 = Coupling flag inputs:
Coupling flag inputs define the flags which are copied from the flag range of the PLC to the DPRAM and thus are provided for visualization. The start flag and the numbers of flags to be transmitted are defined as parameters. The start flag must be within the range of 0 to 255. The number must be selected in such a way that the addition Start flag + Number does not exceed the value 256. If these two conditions are not fulfilled, an error message will be caused.

Block 3: Code CA00 = Coupling flag outputs:
The coupling flags outputs allow a visualization to modify the flags in the flag range of the PLC. For this, it writes the data for the flags in the DPRAM from where they are read by the PLC. The start flag and the numbers of flags to be transmitted are defined as parameters. The start flag must be within the range of 0 to 255. The number must be selected in such a way that the addition Start flag + Number does not exceed the value 256. If these two conditions are not fulfilled, an error message will be caused.

Block 4: Code CC00 = Release DPRAM update:
The parameter of this block determines the data (times, counters, flags etc.) which are written in the DPRAM or read from there. Setting individual bits in this parameter releases the update of the required data. If individual ranges are not selected, the PLC program is processed faster.



Block 5: Code CB00 = Remanent flags:
Definition which flags of the flag range of the PLC shall keep their data after disabling and re-activating the voltage supply. The start flag and the numbers of flags to be remanent are defined as parameters. The start flag must be within the range of 0 to 255. The number must be selected in such a way that the addition Start flag + Number does not exceed the value 256. If these two conditions are not fulfilled, an error message will be caused.

Block 6: Code CB01 = Remanent S flags:
Definition which S flags of the flag range of the PLC shall keep their data after disabling and re-activating the voltage supply. The start flag and the numbers of flags to be remanent are defined as parameters. The start flag must be within the range of 0 to 4095. The number must be selected in such a way that the addition Start flag + Number does not exceed the value 4096. If these two conditions are not fulfilled, an error message will be caused.

Block 7: Code CB02 = Remanent counters:
Definition which counters of the flag range of the PLC shall keep their data after disabling and reactivating the voltage supply. The start counter and the numbers of counters to be remanent are defined as parameters. The start counter must be within the range of 0 to 255. The number must be selected in such a way that the addition Start flag + Number does not exceed the value 256. If these two conditions are not fulfilled, an error message will be caused.

Block 8: Code CD00 = Coupling of several PLCs:
If several SPCs are available in a computer system, it is possible to exchange data between the individual SPCs via the visualization (see chapter "Coupling of several SPC components").
First parameter = data block no.
Second parameter = number of PLCs max. 7
Third parameter = block length of the range max. 32 words

End identification $EEEE_H$

5.1.1 Example data block DB1

DW	0:	KH = 4D41	Header 3 words
	1:	KH = 534B	(MASK01)
	2:	KH = 3031	
DW	3:	KH = CE00	Coupling flag inputs PLC -> visualization
	4:	KF = + 0	First entry start flag
	5:	KF = + 256	Second entry = number
DW	6:	KH = CA00	Coupling flag outputs visualization -> PLC
	7:	KF = + 0	First entry start flag
	8:	KF = + 256	Second entry = number
DW	9:	KH = CC00	Release DPRAM update
	10:	KH = 7FFF	
DW	11:	KH = CB00	Definition of the remanent flags to be stored
	12:	KF = + 50	First entry start flag
	13:	KF = + 10	Second entry = number
DW	14:	KH = CB01	Definition of the remanent S flags to be stored
	15:	KF = + 0	First entry start flag
	16:	KF = + 4096	Second entry = number
DW	17:	KH = CB02	Definition of the remanent counters to be stored
	18:	KF = + 0	First entry start counter
	19:	KF = + 4096	Second entry = number
DW	20:	KH = CD00	Definition of the data coupling between several PLCs
	21:	KF = + 9	First entry = data block no.
	22:	KF = + 7	Second entry = number of PLCs max. 7
	23:	KF = + 32	Third entry = block length of the range max. 32 words
DW	24:	KH = EEEE	End identification

5.2 Status functional module

For status and error messages which do not result in a stop of the PLC, a firmly installed functional module is available. The FB used for this is determined in the file LWLDRV10.INI. This functional module has 7 parameters.

CTR: **Control Byte:** If the 1st bit is set in the control byte, the lightbus master board is induced to restart the lightbus. When the restart has been performed, this bit must be reset.

STA: **Status Byte**: If the restart of the ligthbus requested in the control byte has been performed, this is acknowledged in the status byte by setting the 1st bit. If the 1st bit of the control byte is reset afterwards, the 1st bit in the status byte is reset as well.

ENR: **Error No.:** Provides the error number of the occurred error (see table below).

ERC: **Extended Error Code:** Provides an extended error description (see table below).

SPC **Status Register SPC Hardware**

PB1: **Diagnosis register 1 of the lightbus master component**

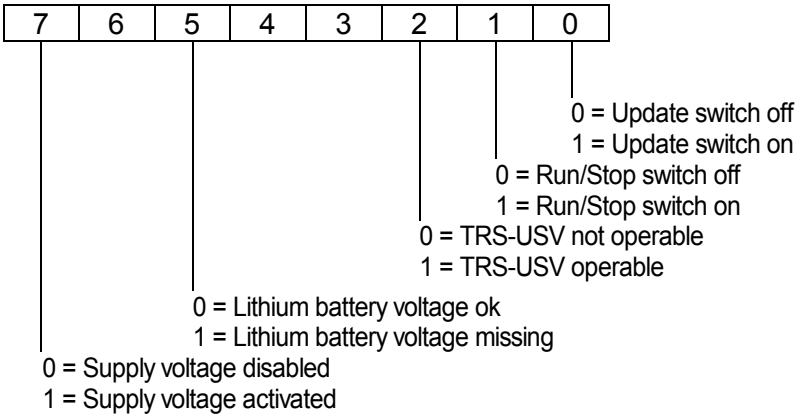
PB2 **Diagnosis register 2 of the lightbus master component**

ENR, ERC: Error table Functional module Error messages:

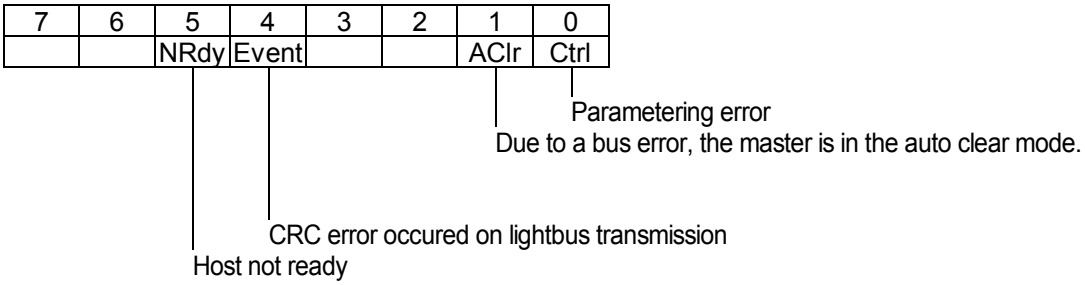
Error Code **ENR**	Extended error code **ERC**	Description
1		Data block DB1 not found
2		Data block DB1 empty
3		Wrong header in DB1
4		DB 1 contains too few parameters or parameters which are not in the valid range.
5		End identification in DB1 not found
6	DB No.	Data block for reading data not found (DB)
7		Offset of the data to be read too big (DB)
8		Number of the data to be read too high (DB)
9	DB No.	Data block for writing data not found (DB)
10		Offset of the data to be written too big (DB)
11		Number of the data to be written too high (DB)
16		Number of the Data block to the SPC coupling too high
17		Number of input ranges too high
18		Number of data words too high
19		Data block with stated number does not exist
20		Length of the data block too low
21	DX No.	Data block for reading data not found (DX)
22		Offset of the data to be read too big (DX)
23		Number of the data to be read too high (DX)
24	DX No.	Data block for writing data not found (DX)

Error Code **ENR**	Extended error code **ERC**	Description
25		Offset of the data to be written too big (DX)
26		Number of the data to be written too high (DX)
30		File PLC43SPC.BIN could not be opened for storage (Step 5 program file)
31		Error in writing in the Step 5 program file PLC43SPC.BIN
40		Lightbus master not ready for warm boot (Ready bit = 0).
41		Lightbus master does not acknowledge the warm boot request within prescribed time (Init bit not 0).
42		Lightbus master does not acknowledge Ready bit within prescribed time
43		Lightbus master does not acknowledge Run bit within prescribed time
44		Lightbus master does not acknowledge Com bit within prescribed time
45		Handshake on transferring data between CM40 and PLC has not been acknowledged within prescribed time.

SPC: Status Register SPC Hardware



PB1: Low byte diagnosis register 1 of the lightbus master component



PB1: High byte diagnosis register 1 of the lightbus master component

This byte represents the main status of the master.

7	6	5	4	3	2	1	0
Ready	Run	Com					

Bit = 1: Data cycles on the lightbus are carried out (lightbus works)

Bit = 1: Lightbus initialization has been carried out

Bit = 1: Firmware of the master component has started correctly

PB2: Diagnosis register 2 of the lightbus master component

Error Code	Description
1	Ring interruption. In the high byte of the diagnosis register is the number of modules which are still transmitting.
2	Overrun of the LWL receiver
3	LWL-CRC error
30	Parametering error of the LWL configuration.
31	CM-40 watchdog has not been triggered within prescribed time.

5.3 USTACK error messages

Error messages which cause a stop of the PLC, are indicated in the USTACK and on the SPC display. The USTACK can be read with the PLC-programmer.

Error messages in the USTACK and in the status display.

Error Code	Extended error code	Description
$E1_H$		File PLC43SPC.BIN could not be opened for loading (Step 5 program file)
$E2_H$		Error on reading from the Step 5 program file PLC43SPC.BIN
$E3_H$		Checksum error on reading the Step 5 program from the file PLC43SPC.BIN
$E4_H$		Step 5 program does not exist in the SRAM memory
$E5_H$		Checksum error on reading the Step 5 program from the SRAM memory
$E6_H$		Lightbus master component not found (no hardware identification).
$E7_H$		Lightbus master component not operable after reset.
FF_H		Temporary voltage loss

5.4 Communication via DPRAM

Division of the DPRAM for communication with a visualization CPU

DPRAM OFFSET	DATA	DIR	Number of bytes
0_H	Times	READ	256
100_H	Counter	READ	256
200_H	Flag	READ	256
300_H	Process image inputs	READ	128
380_H	Process image outputs	READ	128
400_H	Periphery byte inputs	READ	128
480_H	Periphery byte outputs	READ	128
500_H	Coupling flag inputs	READ	256
600_H	Coupling flag outputs	WRITE	256
700_H	Data range Read data block	READ	512
900_H	Data range Write data block	WRITE	512
$B00_H$	Times extended	READ	256
$C00_H$	Counter extended	READ	256
$D00_H$	Q range inputs	READ	256
$E00_H$	Q range outputs	READ	256
1000_H	Communication	READ/WRITE	
1100_H	SPC coupling output data	READ	64
1140_H	SPC coupling input data 1	READ	64
1180_H	SPC coupling input data 2	READ	64
$11C0_H$	SPC coupling input data 3	READ	64
1200_H	SPC coupling input data 4	READ	64
1240_H	SPC coupling input data 5	READ	64
1280_H	SPC coupling input data 6	READ	64
$12C0_H$	SPC coupling input data 7	READ	64
…	…	…	…
1300_H	Fast transfer of 5 data blocks in a SPS-cycle	READ/WRITE	3072
…	…	…	…
$1F00_H$	Component identification		16
…	…	…	…
$1FE0_H$	Semaphores		16
$1FFA_H$	Interrupt selection If and which (ISA)	WRITE	2
$1FFC_H$	Interrupt (PC104)	WRITE	2
$1FFE_H$	Interrupt (ISA)	WRITE	2

5.5 Communication (DPRAM offset 1000H)

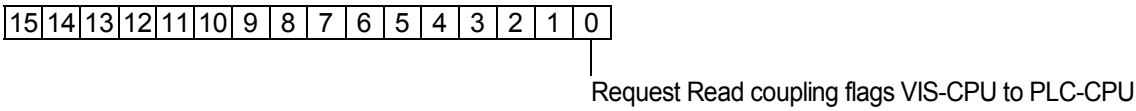
DPRAM OFFSET	FUNCTION
…	…
…	…
1010_H	Request word coupling flag inputs
1012_H	Acknowlegement word coupling flag inputs
1014_H	Request word coupling flag outputs
1016_H	Acknowlegement word coupling flag outputs
…	…
1020_H	Number of the data block for reading data block
1022_H	Offset in the data block for reading data block
1024_H	Number of words to be read from the data block
1026_H	Request word Read data block
1028_H	Acknowledgement word Read data block
$102A_H$	Number of the data block for writing data block
$102C_H$	Offset in the data block for writing data block
$102E_H$	Number of words to be written in the data block
1030_H	Request word Write data block
1032_H	Acknowledgement word Write data block
1034_H	SPC coupling: Output data ready PLC
1036_H	SPC coupling: Reading output data PC
1038_H	SPC coupling: Read input data PC
$103A_H$	SPC coupling: Input data read PLC
$103C_H$	
$103E_H$	
1040_H	Status PLC
1042_H	USTACK error
1044_H	PLC special functions
1046_H	Reset error PLC
1048_H	FB error
$104A_H$	Status Register SPC Hardware
$104C_H$	Diagnosis register 1
$104E_H$	Diagnosis register 2
1060_H	SPS-cycle time in ms

5.5.1 Transmission of the coupling flags

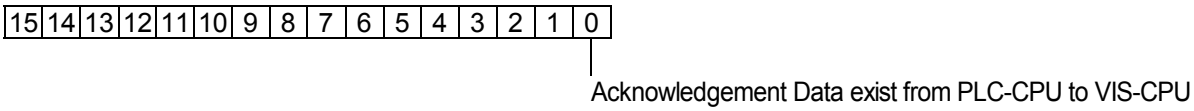
Description of the data transfer Reading coupling flags (inputs):

Set bit 0 in the request word to 1 in order to start data exchange. When the PLC-CPU has copied the data to the DPRAM, it sets bit 0 in the acknowledgement word. Thereupon the VIS-CPU reads the data from the data range "Coupling flags inputs" (DPRAM offset 500_H) and resets bit 0 in the request word to 0 in order to indicate to the PLC-CPU that it has read the data. The PLC-CPU on its part then sets bit 0 in the acknowledgement word back to 0.

Request word Coupling flags Inputs DPRAM offset 1010_H



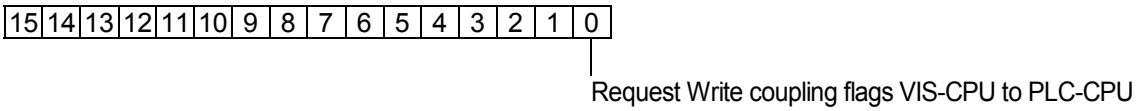
Acknowledgement word Coupling flags Inputs DPRAM offset 1012_H



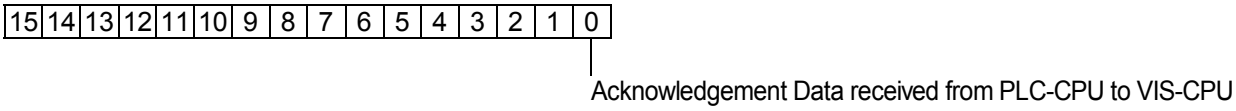
Description of the data transfer Writing the coupling marks (outputs):

First the coupling flags outputs are written in the provided data range (DPRAM offset 600_H).
Then bit 0 is set in the request word. After receiving the data from the PLC-CPU, the latter sets bit 0 in the acknowledgement word. This induces the VIS-CPU to delete bit 0 in the request word, which is then acknowledged by the PLC-CPU by deleting bit 0 in the acknowledgement word.

Request word Coupling flags Outputs DPRAM offset 1014_H



Acknowledgement word Coupling flags Outputs DPRAM offset 1016_H

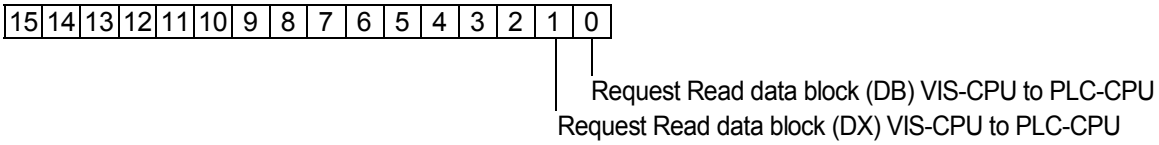


5.5.2 Transfer of a data block

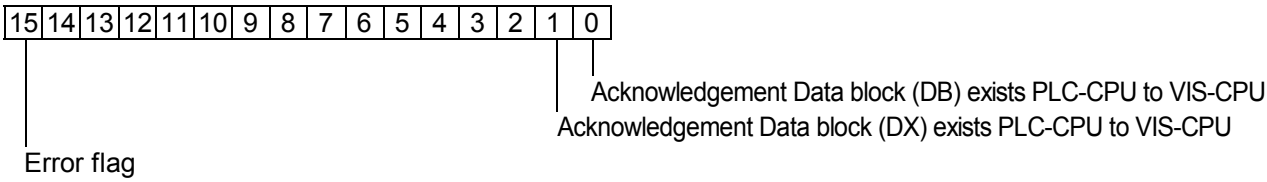
Description of the data transfer Reading a data block (DB or DX):

First the number of the data block, the offset in the data block and the number of the data words to read are written in the DPRAM. Then the bit is set in the request word in order to start data exchange. When the PLC-CPU has copied the data to the DPRAM, it sets the corresponding bit in the acknowledgement word. Thereupon the VIS-CPU reads the data and resets the bit in the request word in order to indicate to the PLC-CPU that it has read the data. The PLC-CPU on its part then resets bit in the acknowledgement word to 0. If an error has occurred while reading a data block, the error flag is set in the acknowledgement bit. The actual error code can then be read in the error word.

Request word Read data block DPRAM offset 1026_H



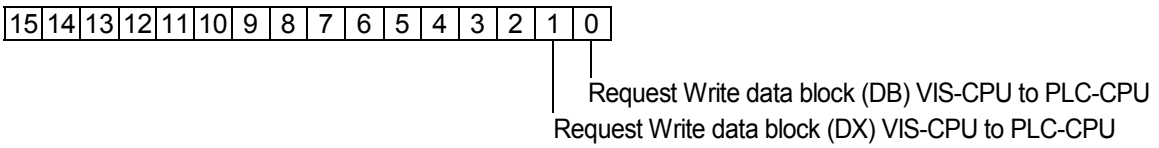
Acknowledgement word Read data block DPRAM offset 1028_H



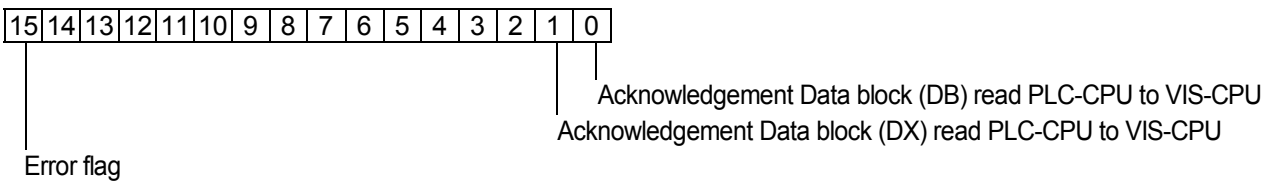
Description of the data transfer Writing a data block (DB or DX):

First the number of the data block, the offset and the number of the data words to write are written in the DPRAM. Then the bit is set in the request word in order to start data exchange. When the PLC-CPU has read the data from DPRAM, it sets the bit in the acknowledgement word. Thereupon the VIS-CPU resets the bit in the request word, which is then acknowledged by the PLC-CPU by deleting the bit in the acknowledgement word.

Request word Write data block DPRAM offset 1030_H



Acknowledgement word Write data block DPRAM offset 1032_H



5.5.3 Coupling of several SPC components

If a system contains several SPC components, it offers the facility that these components can interchange data, if required. For this, the DPRAM contains 8 blocks with 32 words each. One block for output data where the SPC component stores data for other SPCs (transmitting data) and 7 blocks for input data for receiving data from other SPC components.

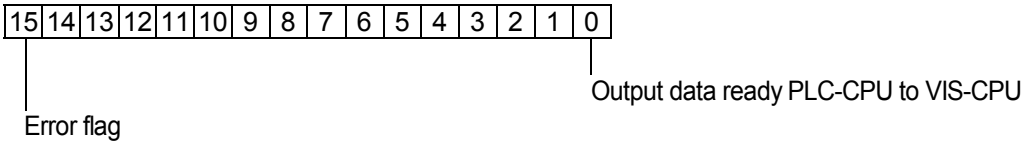
Output data (32 words)
Input data 1 (32 words)
Input data 2 (32 words)
Input data 3 (32 words)
Input data 4 (32 words)
Input data 5 (32 words)
Input data 6 (32 words)
Input data 7 (32 words)

The data to be sent and received are stored in a data block. This data block can be selected in the data block DB 1 itself and must be filled completely before use (e.g. with 0 in all data words). Furthermore, data block DB 1 serves for selecting how many SPCs take part in the data exchange and how many data words are exchanged. Data transfer to the individual SPCs is performed by the higher-level visualization CPU.

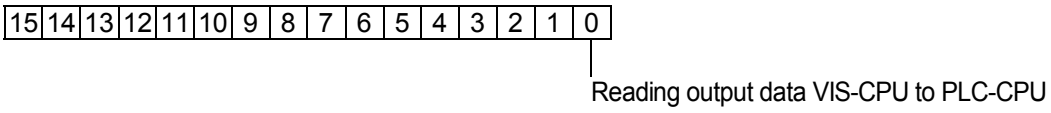
Description Read output data:

The VIS-CPU checks whether the output data are available in the PLC-CPU (Bit 0 = 1 in the word Output data ready). If they are ready, the VIS-CPU can inhibit rewriting of the data by the PLC-CPU by setting bit 0 in the word Reading output data, until it has read all the data. This is necessary to ensure data consistency.

Communication word Output data ready DPRAM offset 1034_H



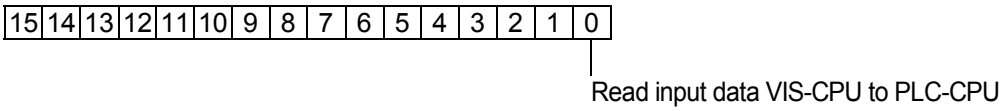
Communication word Reading output data DPRAM offset 1036_H



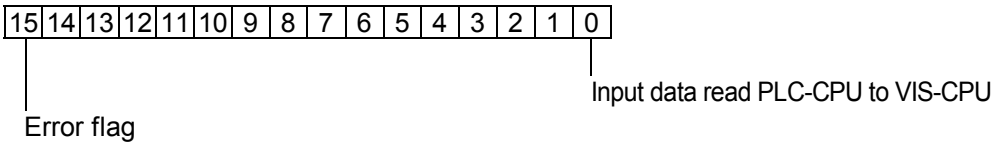
Description Read input data:

The VIS-CPU writes the input data in the DPRAM and sets bit 0 in the communication word Read input data. The PLC-CPU writes the data in the provided data block and acknowledges the receipt of data by setting bit 0 in the communication word Input data read. Thereupon the VIS-CPU recalls its bit, which is acknowledged by the PLC-CPU by recalling its bit.

Communication word Read input data DPRAM offset 1038_H



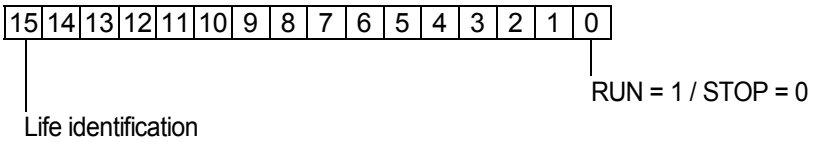
Communication word Input data read DPRAM offset $103A_H$



5.5.4 Status and error messages

Status word of the PLC at DPRAM offset 1040_H

The status word indicates whether the PLC is in state RUN or STOP. Moreover, a bit Life identification is defined. The bit for life identification is set by the PLC-CPU in every cycle. To check whether the PLC is still running, the VIS-CPU sets the bit to 0, then checks if it changes back to 1.



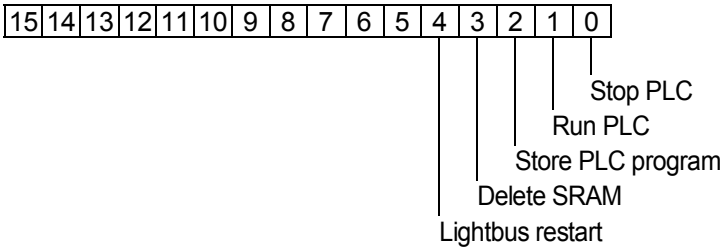
Error word for USTACK errors of the PLC at DPRAM offset 1042_H

All error messages displayed in the USTACK are also output to the dual-ported RAM.
For the corresponding error messages, see table USTACK error messages.
Low byte = Error code
High byte = Extended error code

Special functions of the PLC at DPRAM offset 1044_H

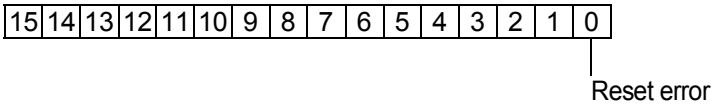
The functions "Stop PLC" and "Run PLC" correspond to the RUN/STOP switch (switch 2) mounted on the hardware. They allow to switch the PLC to Stop and back to the Run state via the DPRAM.
The function "Store PLC configuration" corresponds to the function of the switch Store configuration (switch 1) mounted on the hardware.

The function "Delete SRAM" deletes the SRAM if it is available on the SPC.
The function "Lightbus restart" restarts the Lightbus if the Lightbus communication has been aborted by an error. This function is necessary since the PLC does not switch to the STOP state if an Lightbus error occurs. The same function can be executed via the status FB.



Reset error message at DPRAM offset 1046_H

Resetting the error message by setting bit 0. The PLC deletes this bit after deleting the error message.



Error word for FB error of the PLC at DPRAM offset 1048_H

All error messages output to the status module in the parameters ENR und ERC are also output to dual-ported RAM. For the corresponding error messages, see table Functional module error messages.
Low byte = ENR
High byte = ERC

Status register SPC hardware on DPRAM offset $104A_H$
Diagnosis register 1 on DPRAM offset $104C_H$
Diagnosis register 2 on DPRAM offset $104E_H$

The values of these 3 registers have the same contents as in status FB.

5.5.5 Component identification

The component identification is set in the DPRAM as from the address $1F00_H$ and is defined in blocks with max. 16 byte each as follows:

1. Block:	**SPC-LWL**	**R4.02**	(hardware identification and software version number)
2. Block:	**18.01.1999**		(creation date of the current software version)
3. Block:	**PLC-Ver 1.59**		(software version number of the PLC software)

5.5.6 Transfer of 5 data blocks in a SPS-cycle

In order to achieve a faster transfer, a function has been installed which allows to transfer 5 data blocks in a SPS-cycle. For this, a simplified handshake has been defined. On the normal transfer of data blocks, at least 2 SPS-cycles were needed to transfer a data block.

However, this function has a restriction. In one cycle only 5 data blocks can be read or written, as the data range for the data blocks has to be used for Reading and Writing due to the size of the DPRAM.

Division of the DPRAM memory:

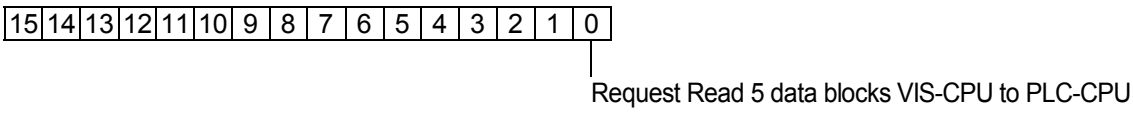
DPRAM OFFSET	FUNKTION
1300_H	Request word Read data block
1302_H	Reserve
1304_H	Request word Write data block
1306_H	Reserve
1308_H	Number first data block. Number = $FFFF_H$ this data block is not used.
$130A_H$	Offset in the first data block
$130C_H$	Number of words to be read or written from the first data block.
$130E_H$	Number second data block. Number = $FFFF_H$ this data block is not used.
1310_H	Offset in the second data block
1312_H	Number of words to be read or written from the second data block.
1314_H	Number third data block. Number = $FFFF_H$ this data block is not used.
1316_H	Offset in the third data block
1318_H	Number of words to be read or written from the third data block.
$131A_H$	Number fourth data block. Number = $FFFF_H$ this data block is not used.
$131C_H$	Offset in the fourth data block
$131E_H$	Number of words to be read or written from the fourth data block.
1320_H	Number fifth data block. Number = $FFFF_H$ this data block is not used.
1322_H	Offset in the fifth data block
1324_H	Number of words to be read or written from the fifth data block.
1500_H	Data range first data block (512 byte)
1700_H	Data range second data block (512 byte)
1900_H	Data range third data block (512 byte)

$1B00_H$	Data range fourth data block (512 byte)
$1D00_H$	Data range fifth data block (512 byte)

Description of the data transfer Reading 5 data blocks:

First the number of the data block, the offset and the number of the data words to read for the 5 data blocks are written into the corresponding addresses of the DPRAM. Then the bit is set in the request word in order to start data exchange. When the PLC-CPU has copied the data to the data ranges of the various data blocks in the DPRAM, it resets the bit in the request word. If an error has occurred while reading a data block, the error flag is set in the acknowledgement bit. The actual error code can then be read in the error word. If less than 5 data blocks are to be transferred, $FFFF_H$ has to be entered into the number of the unused data block

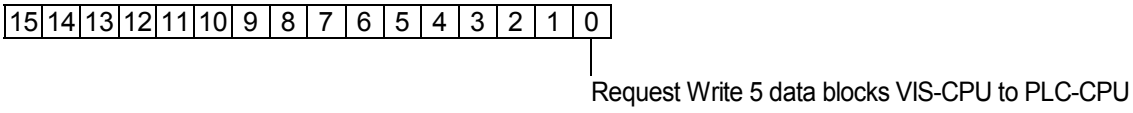
Request word Read data blocks DPRAM-Offset 1300_H



Description of the data transfer Writing 5 data blocks:

First the number of the data block, the offset, the number of the data words to write and the data for the 5 data blocks are written into the corresponding addresses of the DPRAM. Then the bit is set in the request word in order to start data exchange. When the PLC-CPU has read the data from DPRAM, it resets the bit in the request word. If an error has occurred while writing a data block, the error flag is set in the acknowledgement bit. The actual error code can then be read in the error word. If less than 5 data blocks are to be transferred, $FFFF_H$ has to be entered into the number of the unused data block

Request word Write data block DPRAM-Offset 1034_H



6 Configuration of the realtime PLC

The data for configuring the realtime PLC are stored in the file "LWLDRV10.INI" and loaded on starting the program. This file contains an ASCII file and can be edited by means of any editor. However, the indicators in square brackets and the other indicators must not be modified. Modifications may only be performed on the right of the "=" sign.
To modify the file "LWLDRV10.INI", the SPC must be booted in interlink mode.

The file LWLDRV10.INI contains as follows:

```
[UPDATE]
KOPSPC=0
TEILFAKT=10

[SPS]
STATUSFB=10

[HW]
USV=2
SAVEDEST=3
```

KOPSPC: Determines whether a coupling of several SPCs is required or not. If KOPSPC = 1, the coupling interface is processed, otherwise it is not processed.

TEILFAKT: Determines the period in ms in which the cyclic monitoring function is interrupted during an OB1 cycle.

STATUSFB: Determines the functional module which is used for the STATUS FB. This module is available in the SourceCode of the Lightbus driver and should not be overwritten by the PLC.

USV: USV = 0 no NPS.
USV = 1 NPS with power supply unit and accumulator
USV = 2 NPS with TRS NPS power supply unit and SRAM

SAVEDEST: SAVEDEST = 0 PLC program is stored in a flash Eprom during storage
SAVEDEST = 1 PLC program is stored in a flash Eprom during storage
SAVEDEST = 2 PLC program is stored in an SRAM during storage
SAVEDEST=3 PLC program is stored in a flash Eprom and in an SRAM during storage

7 Types of the SPC and their function

7.1 SPC without NPS

In the file "LWLDRV10.INI" for this type, the parameter USV must be 0 and the parameter SAVEDEST must be 0 or 1. If storage for this type was performed in the SRAM, the data would get lost after switching off.

If the SPC is switched on and the realtime PLC is started, the latter checks whether the FLASH-DISK contains a valid PLC program. If so, it loads the program and checks the checksum. If the checksum is OK and the field bus operates properly, the PLC switches to the RUN state.

If the checksum is not OK, an error message is output to the display of the SPC and to the USTACK. The PLC then must be restarted by initial deletion from the programmer and by repeated transmission of the PLC program to the SPC. The RUN/STOP and STORE keys at the SPC are disabled until initial deletion has been executed.

If there is no NPS, the state of the PLC program, which has also been active during the last manual storage, is active again after switching the SPC off and on. This signifies no remanent flags and data block contents.

7.2 SPC with NPS power supply unit and accumulator

In the file "LWLDRV10.INI" for this type, the parameter USV must be 1 and the parameter SAVEDEST must be 0 or 1. If storage for this type was performed in the SRAM, the data would get lost after switching off.

If the SPC is switched on and the realtime PLC is started, the latter checks whether the FLASH-DISK contains a valid PLC program. If so, it loads the program and checks the checksum. If the checksum is OK and the field bus operates properly, the PLC switches to the RUN state.

If the checksum is not OK, an error message is output to the display of the SPC and to the USTACK. The PLC then must be restarted by initial deletion from the programmer and by repeated transmission of the PLC program to the SPC. The RUN/STOP and STORE keys at the SPC are disabled until initial deletion has been executed.

If the PLC program runs and voltage loss is detected, the PLC program is stored in the FLASH disk. This is indicated by the flashing error message "FF" in the status display on the SPC. Storage takes approx. 6 sec. For this type, however, please note that the PLC program is not stored on switching off the computer regularly via the mains switch of the computer power supply unit.

For this NPS type, the state of the PLC program, which has also been active during the last manual storage, is also active again after switching the SPC off and on. This signifies no remanent flags and data block contents. If flags and data block contents shall be remanent, the computer must not be switched off via the switch of the computer power supply unit.

7.3 SPC with TRS NPS power supply unit

In the file "LWLDRV10.INI" for this type, the parameter USV must be 2 and the parameter SAVEDEST must be 2 or 3.

If the SPC is switched on and the realtime PLC is started, the latter checks whether the SRAM contains a valid PLC program. If so, it loads the program and checks the checksum. If the checksum is OK and the field bus operates properly, the PLC switches to the RUN state.

If the checksum is not OK, an error message is output to the display of the SPC and to the USTACK. The PLC then must be restarted by initial deletion from the programmer and by repeated transmission of the PLC program to the SPC. The RUN/STOP and STORE keys at the SPC are disabled until initial deletion has been executed.

If there is no program in the SRAM, an error message is also output to the display of the SPC and to the USTACK. However, it is now possible to reload the program from the FLASH disk. Of course, the prerequisite for this is that the parameter SAVEDEST is set to 3. If not, there is no PLC program on the FLASH disk.

To reload from the FLASH disk, press the Reload Flash key and actuate the memory switch from left to right and back 3 times within 6 seconds. The Reload Flash key must be actuated during the whole reload procedure.

If a reading error or a checksum error is detected on loading from the FLASH disk, an error message is output; then proceed in the same manner as for an SRAM checksum error.

If no program is found in the SRAM nor on the FLASH disk, it must be transmitted from the programmer again.

If the PLC program runs and voltage loss is detected, the PLC program is stored in the SRAM. This is indicated by the flashing error message "FF" in the status display on the SPC. Storage takes approx. 300 msec. For this type, storage is also performed on normally switching off the computer by the mains switch of the computer power supply unit. Flags and data block contents are remanent for this type, provided that the flags to be kept remanent are configured in the DB 1.

The TRS NPS power supply unit requires a charging time of 1.5 minutes to ensure sufficient load for buffering. If a voltage loss or switching off occurs within these 1.5 minutes after switching on the SPC, no storage is performed.

7.4 Manual storage

There are 3 ways to store the PLC program on the FLASH disk or in the SRAM manually.

1. Storage via the memory switch at the SPC.
2. Storage via the dual-ported RAM by setting the corresponding bit in the word "Special functions of the PLC" at DPRAM offset 1044_H
3. Storage via the programmer. For storage via the programmer, the PLC must be set in the STOP state, then compression must be started. The PLC program is then compressed and stored afterwards.

8 Hardware description SPC base board

(Dual-ported RAM module for installation of a slave PC in an ISA system)

8.1 General information

The SPC-XXX is a PC plug-in board. It serves mainly for separating a PC-104 CPU and a PC-104 field bus interface from the ISA bus by means of a dual-ported RAM. Furthermore, it provides various periphery functions for the PC-104 bus, which are described in the following chapters.

8.2 Functions of the board

The board contains the following functions:

- 2 pcs. PC-104 interfaces for plugging the local CPU and other PC-104 components.
- Dual-ported RAM coupling between ISA bus and local CPU optionally with 4K*16bit or 8K*16bit dual-ported RAM. The dual-ported RAM begins at the address D000:0000. From the outside (ISA BUS), the address range can be adjusted via a hex switch at the top of the board. The interrupt and semaphore logic of the dual-ported RAM is decoded.
- Register for determining the dual-ported RAM interrupt on the ISA bus
- 1 MB buffered SRAM, divided into 32 pages with 32 KB each
- OWG master interface
- CAN master interface
- COM1 and COM2 of the plugged PC-104 CPU are lead through sub-D plugs.
- NPS power supply unit logic
- Battery connection for external battery via NPS port
- Voltage monitoring of the NPS battery
- Voltage monitoring of the external battery
- Switch for Run/Stop and update function
- Reset key for local reset
- 2 pcs. 7-segment display for indicating diagnosis, operation and error messages
- Timer for triggering an NMI on the local CPU and, if required, also on the ISA bus

8.3 Addresses on the ISA bus

As standard, a DP-RAM of 8KB organized with 4K*16bit is mounted on the module. The address range of the ISA page can be displaced in 8 steps of 8K by means of the hex switch S200 on top of the module. The upper addresses of the DP-RAM dispose of special functions (see table below).

Switch position	Normal address range	Set INT (Wr) to PC-104 CPU	Clr INT (Rd) from PC-104-CPU	ISA interrupt select
0	D0000H..D1FDFH	D1FFCH	D1FFEH	D1FFAH
1	D2000H..D3FDFH	D3FFCH	D3FFEH	D3FFAH
2	D4000H..D5FDFH	D5FFCH	D5FFEH	D5FFAH
3	D6000H..D7FDFH	D7FFCH	D7FFEH	D7FFAH
4	D8000H..D9FDFH	D9FFCH	D9FFEH	D9FFAH
5	DA000H..DBFDFH	DBFFCH	DBFFEH	DBFFAH
6	DC000H..DDFDFH	DDFFCH	DDFFEH	DDFFAH
7	DE000H..DFFDFH	DFFFCH	DFFFEH	DFFFAH

8.3.1 Terms

Normal address range
This range is the normal DP-RAM.

INT
If this address (word) is described by the ISA bus, an interrupt is triggered on the PC-104 CPU. The prerequisite is that an interrupt is activated by bridge and the corresponding interrupt is released (see bridge assignment). The interrupt is deleted by the PC-104 page by reading the same cell. Furthermore, the address disposes of a normal DP-RAM function.

Clr INT
By reading this address, an interrupt generated by the PC-104 bus is reset. The interrupt must be activated by describing the ISA interrupt select address and released in the interrupt controller, so that it becomes active on the ISA bus (see below). Furthermore, the address disposes of a normal DP-RAM function.

ISA interrupt select
It is possible to select by writing a data word in this address if and which interrupt from the DP-RAM is generated on the ISA bus. After a reset, the interrupt is disabled.

Data word	Interrupt
0	IRQ 5
1	IRQ 7
2	IRQ 9
3	IRQ 10
4	IRQ 11
5	IRQ 12
6	IRQ 15
7	disabled

8.4 Functions on the local PC-104 bus

8.4.1 Memory addresses on the local PC-104 bus

As standard, the memory address ranges on the local bus cannot be displaced. However, they can be modified by reprogramming a PAL. Optionally, displacement by bridges is also possible.

8.4.1.1 DP-RAM

The upper addresses of the DP-RAM dispose of special functions (see table below)

Normal address range	Set INT (Wr) to ISA-CPU	Clr INT (Rd) from ISA-CPU
D0000H..D1FDFH	D1FFEH	D1FFCH

8.4.1.1.1 Terms

Normal address range
This range is the normal DP-RAM.

Set INT
If this address (word) is described by the PC-104 bus, an interrupt is triggered on the ISA CPU. The prerequisite is that the ISA interrupt select is defined and the corresponding interrupt is released. The interrupt is deleted by the ISA page by reading the same cell. Furthermore, the address disposes of a normal DP-RAM function.

Clr INT
By reading this address, an interrupt generated by the ISA bus is reset. The interrupt must be activated by mounting the corresponding bridge and released in the interrupt controller, so that it becomes active on the PC-104 bus (see bridge assignment). As standard, the bridge for IRQ9 is installed. Furthermore, the address disposes of a normal DP-RAM function.

8.4.1.2 Buffered SRAM

A buffered SRAM with 1 MB is implemented on the module. It is divided into 32 pages with 32 KB each. The page address is written in the I/O address 228H. The buffering battery is external and connected to the NPS port (see chapter NPS port). The battery voltage can be monitored by reading an I/O address (see below). The access to the RAM is locked after a fall of the 5 V supply below 4.6 V.

Addresses:	Memory address	D8000H..DFFFFH
	Page address	I/O 228H

8.4.2 I/O functions on the local PC-104 bus

8.4.2.1 Display port (Wr I/O 78,79,80)

The SPC-XXX disposes of a 2-digit 7-segment display. On booting, it is described on the I/O port 80 and displays the diagnosis information of the BIOS. Since this address is also used as DMA page register by the BIOS, the display address should be switched to port 79 by writing the control byte in port address 223 with set bit D4 (see 7.4.2.2) after booting. The operating state of the module can then be displayed via this display address. The HEX value written in the display address is always displayed hereby. If the superior half-byte of the transmitted value is 0, the corresponding digit is disabled. An error message can be additionally output via a second display address at port 78. If a byte with set bit D7 is written in this address, the display switches between the two displayed values in intervals of 2 seconds.

Function	Address	Date
Control byte	Wr I/O 223H	xxx0 xxxx BIOS diagnosis is displayed (default after reset) xxx1 xxxx Operating state is displayed
BIOS diagnosis	Wr I/O 80H	xxxx xxxx Hex date is displayed directly
Operating state	Wr I/O 79H	xxxx xxxx Hex date is displayed directly
Error message	Wr I/O 78H	0xxx xxxx Error message without function 1xxx xxxx Error message and operating state or BIOS diagnosis are displayed alternately.

8.4.2.2 Port for page address SRAM

Function	Address	Date
Page address	Wr I/O 228H	00H .. 1FH defines 32 K page of the SRAM

8.4.2.3 Status port

Various states can be inquired on the module via the status port.

Function	Address	Date
Status port	Rd I/O 234H	xxxx xxxx |||| ||||_ 0 = Update switch disabled |||| ||| 1 = Update switch activated |||| ||| |||| ||__ 0 = Run switch disabled |||| || 1 = Run switch activated |||| || |||| ||___ not assigned |||| | |||| |____ not assigned |||| ||||_____ not assigned ||| |||_____ 0 = Cmos battery voltage ok || 1 = Cmos battery voltage missing || ||_____ not assigned | |_____ 0 = Mains voltage disabled (NPS operation) 1 = Mains voltage activated

8.4.2.4 RESET key

By pressing the Reset key S400, a local reset can be generated for the PC-104 CPU. The reset signal is not transmitted to the ISA bus.

8.4.2.5 RUN and UPDATE switch

The two switches S401 and S402 can be read via the status port (chapter 7.4.2.3). If the PC-104 is applied in an SPC-XXX, they are used for the RUN/STOP or UPDATE function.

8.4.2.6 CMOS battery voltage

The buffered SRAM and the clock at the local CPU require an external battery supply of 3V. The voltage is connected to pin X401 (see pin assignment). If a system disposes of several SPC components, the battery voltage can be distributed to all modules via a flat conductor cable. The CMOS battery voltage is monitored. When it falls below 2.8V, the corresponding bit in the status port switches to High. If the buffered RAM or the CMOS clock is not required, it is not necessary to connect the battery. The setup of the local CPU is stored in the flash.

8.4.2.7 NPS control

In a system where data must be stored in case of voltage loss and the buffered SRAM cannot be used for this (e.g. in the SPC-XXX), storage can be performed with an NPS system. In this case, the computer must be equipped with an NPS power supply unit and wired according to Fig. 2.

If voltage supply fails, the accumulator of the NPS power supply unit takes over the system supply and generates a power-fail signal, which can be read from the status port bit 0 (polling). If the signal is activated, the local CPU saves all critical data in a non-volatile storage (e.g. Silicon disk) and switches the NPS power supply unit off via the NPS control address.

If critical data from the system master (CPU on ISA bus) must also be saved, the corresponding power-fail message and the RDY message can be output via the DP-RAM.

Some NPS power supply units create a warning signal if the accumulator is not charged completely. The corresponding state can be read in the status port (see chapter 6.4.2.3).

Function	Address	Date
NPS ctrl address	Wr I/O 235H	Bit 0 = 1 Disable NPS supply

8.4.2.8 NMI timer

Windows applications do not allow to generate an exact time-slot pattern via a normal timer function. Therefore, the SPC component disposes of a timer which creates NMIs in an adjustable time-slot pattern. If 0 is written in the corresponding register, the function is disabled (default after reset).

Inserting the bridge B403 activates the NMI on the ISA bus as well.

Function	Address	Date
Page address	Wr I/O 237H..238H	0000H = NMI timer disabled xxxxH = NMI time in

8.4.2.9 II/O interface

As standard, the II/O master interface is integrated in the IO range. Optionally, the interface can also be placed in the MEM range.

The intensity of the OWG transmitter can be modified via the switch S601. If the LED LD600 is flashing, transmission is performed with high intensity. When using OWG cables which are shorter than 15m, low intensity should be activated. Then the LED LD600 is dark.

Function	Address	Date
	I/O 280H .. 29FH	

9 Appendix

9.1 Pin assignments keyboard:

Pin	Designation
1	Keyboard clock
2	Keyboard data
3	NC
4	GND
5	+5V

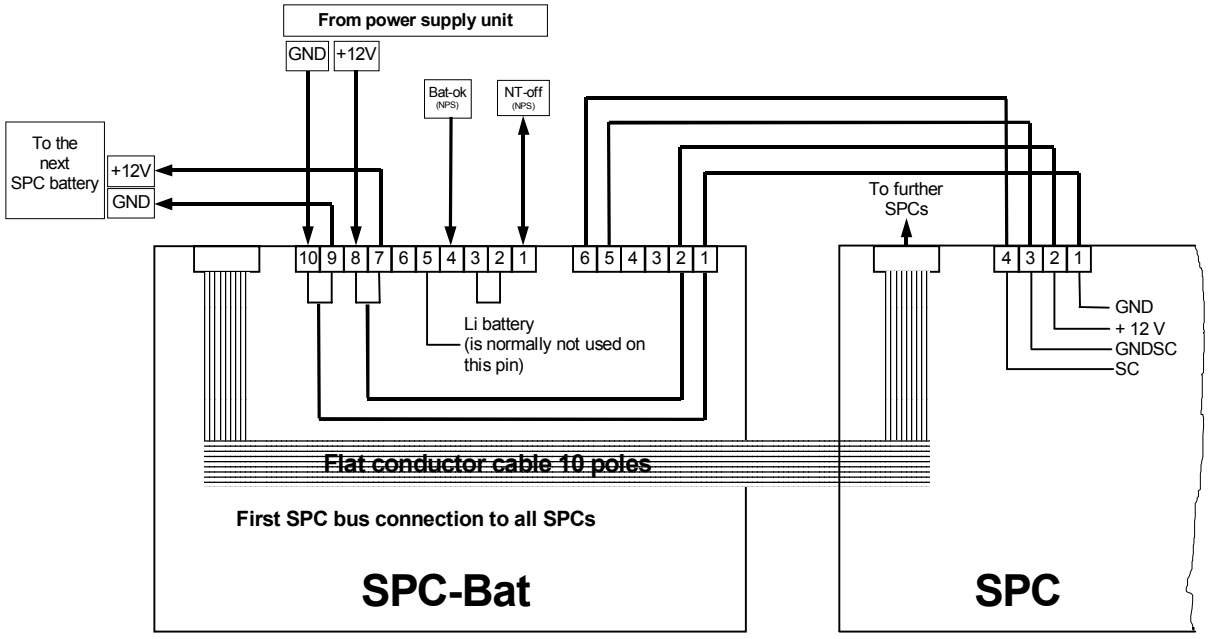
9.2 Pin assignment zero modem cable

The zero modem cable requires a 9-pole SUB-D plug (jack) which must be connected as follows.

Designation	Pin
CD	1
RXD	2
TXD	3
DTR	4
GND	5
DSR	6
RTS	7
CTS	8
R	9

Pin	Designation
1	CD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	R

9.3 Wiring diagram TRS NPS power supply unit



Attention:
The signals nominated NPS are only used if an NPS power supply unit is available. Bat-Ok can only be read before the first SPC. The power supply unit is disabled before the first SPC (via software handshake internally in the DP-RAM).

9.4 Various installation possibilities of a SPC

Note:
The subsections "Used components:" each list the components that are suitable for the corresponding installation type. In the listed numbers the number parts which are not relevant in this connection are described as x.

9.4.1 SPC without data remanence

9.4.1.1 Standard installation

If the SPC does not need any data remanence, supplementary wiring operations are not necessary. In this case, the SPC gets its supply voltage via the ISA bus.

Caution:
You have to use a SPC without data remanence for this operation mode.

9.4.1.1.1 Used components:

SPC-xxx-xx

9.4.1.2 SPC in the PC with external voltage supply

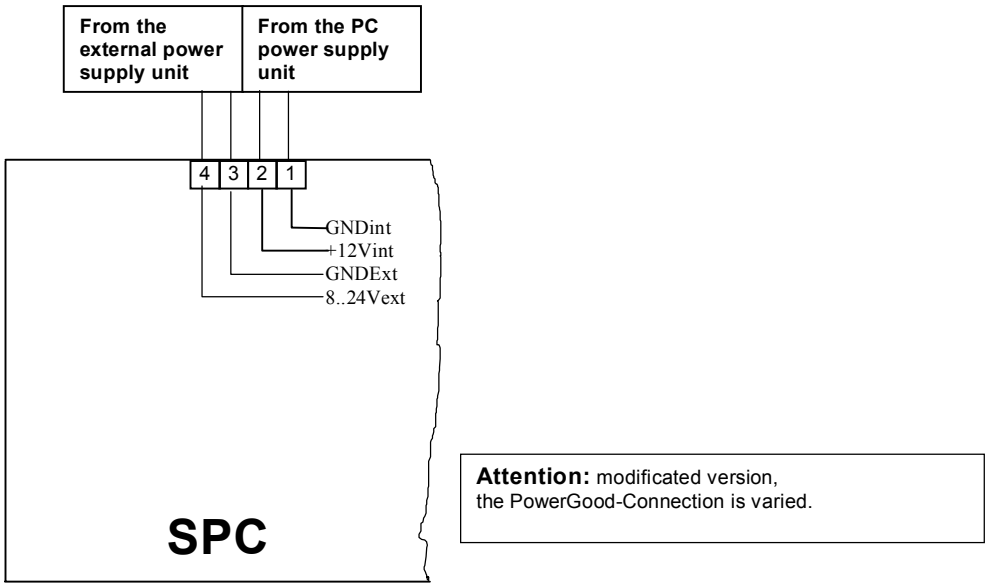
Some applications require that the SPC remains in operation even if the PC is switched off. In this case, a SPC version for 24-V operation is used (modificated version). Then the internal 12 V of the PC as well as the external 24-V supply are connected to the SPC. The SPC is in operation if either the PC is running or the external 24 V are connected. Both supply voltages are separated to each other with diodes.

Caution:
The internal 12 V of the PC have got to be connected in this case because the SPC must not be without voltage as long as the ISA bus is supplied.

That the SPC does not save when switching off the PC, the memory variables in the file ‘D:\xxxdrv10.ini’ have to be defined as follows:

NPS=0
SAVEDEST=1

9.4.1.2.1 Connection diagram



9.4.1.2.2 Used Components:

SPC-xxx-xx-0-P

9.4.2 SPC connections with data remanence

(Saving the whole operating time data when switching off the system.)

In order to save the remanent data of a SPC in case of power failure, a SPC-Bat or a NPS power supply unit can be used. In the following, the different possibilities are described.

9.4.2.1 SPC in a PC with NPS power supply unit

If the SPC is installed into a PC with NPS power supply unit, a SPC version without data remanence is used. The power supply of these versions occurs via ISA bus. In case of a failure of the primary voltage, the PowerGood-Signal of the power supply unit indicates “false“. Then the SPC saves the remanent data in the internal flash memory. As soon as the memory process is complete, the SPC switches off the power supply unit via line NT-Off.
In order to reach this mode of operation of the SPC it is necessary to define the memory variables in the file ‘D:\xxxdrv10.ini’ as follows:

NPS=1
SAVEDEST=1

The control lines of the NPS power supply unit (TRS PC) are connected to the 10-pole ribbon cable plug as follows:

Pin	Function	Colour NPS control line
1	N.C.	
2	N.C.	
3	/NT-Off	brown
4	PowerGood	red
5	NPS-Link	
6	LiBattery	
7	GND	black
8	GND	
9	N.C.	
10	N.C.	

9.4.2.1.1 Used components:

SPC-xxx-xx

9.4.2.2 Several SPCs in a PC with NPS power supply unit

In this case the functional memory sequence is the same as when using one SPC. A SPC version without data remanence is used here as well. However, the following points must be considered for wiring.

The PowerGood-Signal of the power supply unit is connected parallel to all SPCs.
The NT-Off-Signal of the SPCs must not be connected parallel, or the SPC will switch off the NT which has finished saving first.
Therefore the SPCs are connected to the line 'NPS-Link'. The NT-Off-Signal is connected from only one SPC to the power supply unit. In this combination, the FPGA makes sure, that the SPC which finishes saving last will switch off the power supply unit.

This NPS Link-function is available from the following FPGA versions onwards:

For the printed board index _ **104SLVA dated 03.07.1998**
For the printed board index C **104SLVCA dated 07.10.1998**

In this case the memory variables in the file 'D:\xxxdrv10.ini' have also to be defined as follows:

NPS=1
SAVEDEST=1

The control lines of the NPS power supply unit (TRS PC) are connected to the 10-pole ribbon cable plug of the SPC as follows:

Pin	Function	SPCn	SPC3	SPC2	SPC1	Colour NPS control line
1	N.C.					
2	N.C.					
3	/NT-Off				----------	--------brown
4	PowerGood	----------	---------- -	---------- -	---------- -	----------red
5	NPS-Link	---------- -	---------- -	---------- -	---------- -	
6	LiBattery					
7	GND	---------- -	----------	---------- -	---------- -	--------black
8	GND	----------	---------- -	---------- -	---------- -	
9	N.C.					
10	N.C.					

9.4.2.2.1 Used components:

SPC-xxx-xx

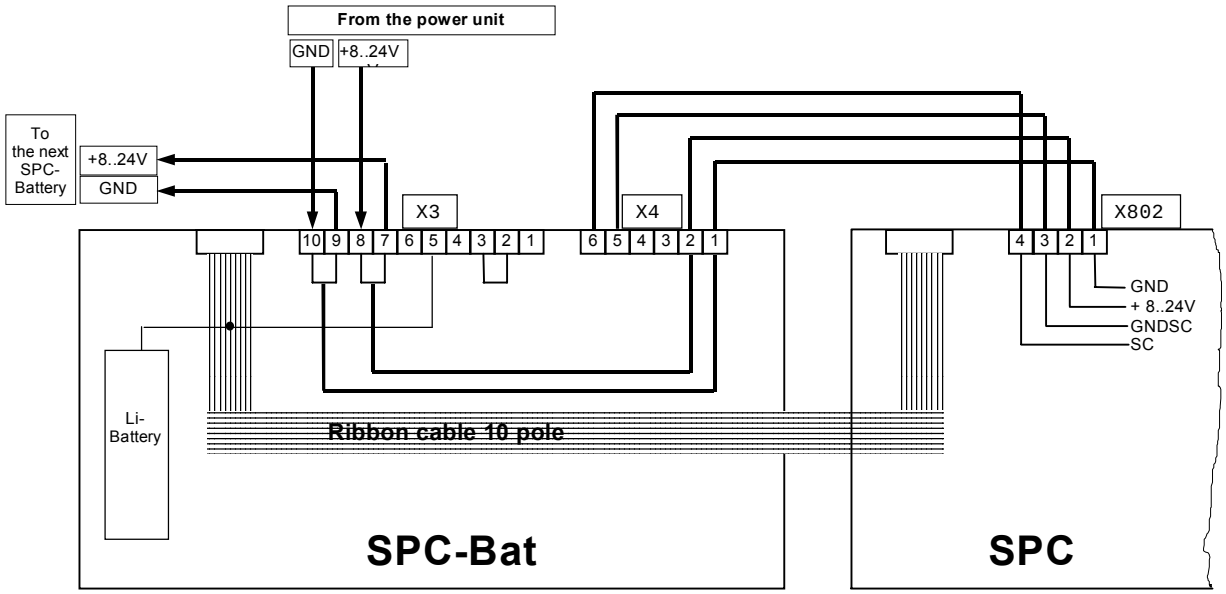
9.4.2.3 SPC with data remanence

The SPC versions with data remanence consist of 2 modules, of the real SPC component and the SPC-Bat. In this case the SPC is not supplied with the 5 V of the ISA bus but with 8 – 24 V, in the PC typically with + 12 V. For this, the power supply and all signals required by the power supply unit are connected to the connector X3 of the SPC-Bat. The connection of the control signals from the SPC-Bat to the SPC occurs via a 10-pole ribbon cable. The power supply and the accumulator voltage are transferred from connector X4 of the SPC-Bat to connector X802 of the SPC via 4 lines with a minimum cross-section of 0.5.
From nov./98 onwards the failure of the primary voltage is not indicated any more with the signal PowerGood, but with a voltage supervision on the SPC-Bat module (**Caution:** From this version onwards it is not necessary any more to connect the PowerGood-Signal of the PC).
Then the communication to the ISA bus is interrupted and the supply of the SPC is taken over for about 3s by the SPC-Bat. During this time the data to be rescued are copied into the buffered SRAM of the SPC. Therefore the memory variables in the file 'D:\xxxdrv10.ini' have to be defined as follows:

NPS=2
SAVEDEST=3

As the buffer battery for the SRAM is on the SPC-Bat, the data of the SRAM are lost for a bit more than a minute when the ribbon cable is removed.

9.4.2.3.1 Connection diagram



9.4.2.3.2 Used components:

SPC-xxx-xx-R

9.4.2.4 SPC with data remanence and additional external power supply

Some applications require that a SPC with data remanence remains in operation even if the PC is switched off. In this case, a modificated SPC-Bat is used (see "Used components:"). Then the internal 12 V of the PC as well as the external 24-V supply are connected to the SPC-Bat. The SPC is in operation if either the PC is running or the external 24 V are connected. Both supply voltages are separated to each other with diodes.

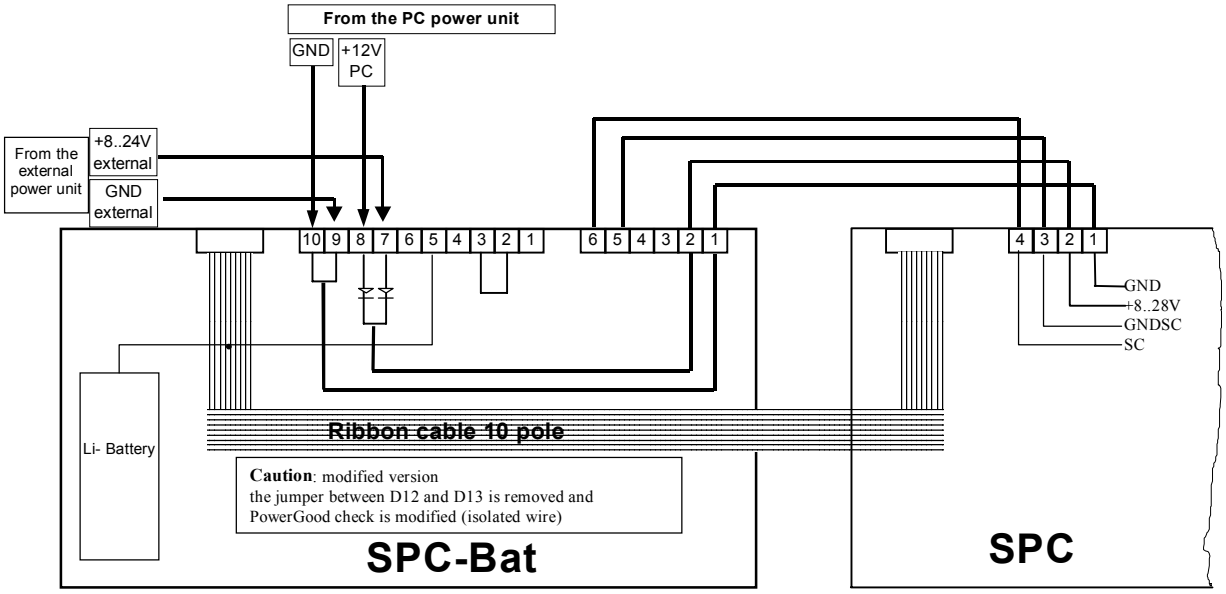
Caution:
The internal 12 V of the PC have got to be connected in this case because the SPC must not be without voltage as long as the ISA bus is supplied.

That the SPC does save when switching off the PC, the memory variables in the file 'D:\xxxdrv10.ini' have to be defined as follows:

NPS=2
SAVEDEST=3

As the buffer battery for the SRAM is on the SPC-Bat, the data of the SRAM are lost for a bit more than a minute when the ribbon cable is removed.

9.4.2.4.1 Connection diagram



9.4.2.4.2 Used components:

SPC-xxx-xx-R-P

9.4.2.5 General installation notes

As it is sometimes difficult to tap the 5-V supply in a PC, two adapters are enclosed in the standard accessory of the SPC-Bat. With help of these a cable can be connected to an existent connection without interrupting it. The connection of the power supply can also occur with the two enclosed cable connectors at the screw terminals of the system bus.

If the SPC-Bat is installed into a MIPCH of TRS, it can be attached to the right side panel with the enclosed threaded bolts.

On the SPC-Bat the switches, keys and 7-segment displays of the SPC are led onto the slot plate. These components may be connected to the SPC with the enclosed 26-pole ribbon cable, for example if the SPC is installed into a 19‘‘ PC. But then it is necessary to put the keys "Reset" and "Load" on the SPC out of operation by disconnecting of the middle connection pin.

Caution:
In this case the SPC has got to be connected to the SPC-Bat with the 26-pole ribbon cable, or the SPC will receive a continuous reset due to the disconnected Reset key. Besides, both switches of the SPC must be on position "PLC" or "Run" in that case.